SCRIBE

Video Text Generator

MAINTENANCE MANUAL

PeLL (Pelligreno) Alumni

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Section 1

GENERAL INFORMATION

1.1 ABOUT THIS MANUAL

The technical manual is organized to provide the maintenance technician with an overview of the SCRIBE system, functional descriptions of major subassemblies, diagnostic information and instructions, video alignment procedures, and preventive/special maintenance procedures. The seven sections of this manual are organized as follows:

Section 1, Introduction, also provides installation and initial adjustment procedures, as well as instructions for modifying the Drive Configuration Table when adding or removing disk drives, tape drives, or controllers to/from the system.

Section 2, System Overview, contains an overall description of the system and its major subassemblies. This section also contains information regarding operational error logging and boot-PROM error codes. Therefore, this section is a useful place to start when initially diagnosing system errors.

Section 3, SCRIBE Detailed Theory of Operation, provides detailed theory of operation and block diagrams for all system subassemblies.

Section 4, SCRIBE Diagnostics Operation, provides detailed, step-by-step instructions for how to operate the SCRIBE diagnostic program and how to interpret results through a complete list of error responses. This section also provides instructions for board removal and shipping.

Section 5, Video Alignment, provides step-by-step adjustment and alignment procedures for all versions of the Sync Gen and Encoder boards used in the SCRIBE system.

Section 6, Operational Maintenance Procedures, provides scheduled maintenance procedures for the system. These include step-by-step instructions for how to replace the lithium cell used for battery backup and the fuse used for the SCSI bus, both of which are located on the CPU board.

Section 7, Schematic Catalog, contains a listing of available schematic diagrams and their CHYRON part numbers for ordering.

1.2 SYSTEM OVERVIEW

The SCRIBE system is a high-resolution video text generator that can display an almost unlimited variety of typestyles with a resolution that approaches the theoretical maximum for character generators. The SCRIBE uses advanced anti-aliasing techniques to create text with the same high quality as that of metal-foundry cast type used in the letterpress industry.

1.2.1 MAINFRAME

The SCRIBE system is based on the 68010 multi-processor chip, and uses the VME/VMX bus specifications for most internal data transfer and control. The main electronics chassis includes the following subsystems:

- 68010 MPU
- Bipolar Microprocessor Unit (BMPU)
- Font Memory Circuitry (w/ up to 2.0 MBytes RAM)
- Frame Buffers (A, B, C, D)
- Display and Cursor Subsystem
- Disk Controller
- Sync Generator with Genlocking
- Encoder (available in NTSC, PAL or component RGB)
- Keyer/Fader
- 20 MByte Winchester-type Hard Disk Drive
- 1.2 Mbyte Floppy Disk Drive
- Power Supplies

1.2.2 KEYBOARD

The SCRIBE uses a separate keyboard, which contains its own power supply. The keyboard supports a daisy-chain interface, allowing additional keyboards to be used with the system. Loop-through relays on each keyboard delegate control to the powered-on keyboard closest to the SCRIBE mainframe. The keyboard also contains a separate address keypad with a four-digit LED readout. The keyboard uses 115VAC/60 Hz (230VAC/50 Hz optional).

1.3 SCRIBE PHYSICAL DIMENSIONS

1.3.1 MAINFRAME

Height: 19-1/4 inches
Width : 19 inches
Depth : 22 inches

1.3.2 KEYBOARD

Height: 4-3/4 inches
Width : 21-1/4 inches
Depth : 11-3/4 inches

1.4 SYSTEM POWER CONSUMPTION

- MAIN CHASSIS: 900 watts maximum.
- KEYBOARD: 125 watts maximum.

1.5 DELETED

1.6 DIAGNOSTIC/TROUBLESHOOTING APPROACH

This manual provides the maintenance technician with a functional understanding of the SCRIBE system. The qualified technician will then be able to perform routine periodic maintenance, isolate difficulties to individual circuit boards, or (in some cases) to particular serviceable components, and either repair the board or replace the damaged board with a functional one.

Maintenance procedures are based on an in-circuit diagnostic program group and complete error logging utility, and are designed to allow the technician to restore system operation with a minimum of downtime.

The technician should have an advanced understanding of electronic circuits and standard test equipment, and be familiar with good technical practices including anti-static precautions.

Most circuit failures can be isolated to one of the SCRIBE's subsystems, which are located on circuit cards within the mainframe. A faulty circuit board can be swapped with a working board to restore operation as quickly as possible.

However, in certain cases involving memory subsystems (Frame Buffers, Dual Ported Memory [font memory]), the diagnostic program will label "suspect" chips through decoding failing addresses. Please note that there are often several factors that will cause a chip to be posted as "suspect", such as RAS*/CAS* failures, address latch failures, stuck address/data bits, etc. The only clue to the actual failure is in the pattern of the failure, including the locations, addresses, and numbers of failures per chip. Therefore, you should contact CHYRON Customer Service immediately upon encountering such a situation.

CAUTION

If you attempt to replace a chip on any SCRIBE circuit board without the assistance of CHYRON Customer Service, you will void your warranty!

1.7 INSTALLATION

This paragraph contains instructions for installing the SCRIBE system into your studio environment. The installer should have a knowledge of basic studio set-up before proceeding.

1.7.1 UNPACKING THE SYSTEM

The SCRIBE system is shipped in three cartons; one contains the SCRIBE mainframe, one contains the keyboard console, and the third contains documentation and logics. Unpack the system as follows:

1. Remove and retain packing lists from sides of cartons.
2. Open cartons as indicated on "THIS SIDE UP".

NOTE

> You should store all packing material in case it is needed for future shipments.

3. Remove all packing materials from cartons, being careful not to damage system components.
4. Remove all components and accessory material, and check against packing list. If you discover anything damaged, contact the shipping firm and file a damaged-material claim. If there are any components or accessories missing, immediately contact the CHYRON Customer Service Department and report the missing items.

1.7.2 RESHIPMENT

If it is ever necessary to reship the SCRIBE system, we recommend that the original packing material be used. Note that you must contact the CHYRON Customer Service Department and obtain a Material Return Authorization (MRA). Also, the shipping containers should be marked in accordance with the directions on the MRA form.

1.8 SYSTEM INTERCONNECTIONS

All inputs and outputs for the SCRIBE system are made to and from connectors on the rear panel (backplane) of the SCRIBE mainframe (Figure 1-1).

1.8.1 VIDEO INPUTS

- PROGRAM IN is the source video from the studio, tape machine, etc., that the SCRIBE is to generate text over. This input is used as a timing reference in the factory configuration.

- REFERENCE IN is normally unconnected when the SCRIBE is shipped. Usually, J20 (REF VIDEO) on the Encoder Board is connected to J3 on the Analog Transition Board, which feeds the signal to the Sync Generator Board. In this configuration, the SCRIBE uses the PROGRAM IN signal to generate its own internal reference. Many broadcast stations and edit facilities use a reference signal, such as black burst, as a genlock source to ensure all equipment is in synchronization.

  Refer to Paragraph 1.9, System Setup and Adjustments, for the procedure for changing the reference video setup.

1.8.2 VIDEO OUTPUTS

- ENCODER OUTPUTS involve the encoder section of the Encoder board.

1.8.2.1 Color Edit. COLOR EDIT shows SCRIBE generated characters and backgrounds, along with the safe title area marker and cursor/tab markings. It is useful for operators to monitor this output for use as a guide while creating graphics.

- VIDEO1 and VIDEO2 are similar to COLOR EDIT, but do not carry the safe title boundaries or cursor/tab markings. These outputs are generally used for upstream configurations.

- DLY KEY (delayed key) is the KEY signal timed to VIDEO1 and VIDEO2 outputs. Note that this is an analog key and is meant to operate in conjunction with a linear type keyer.

1.8.2.2 Keyer Outputs. Keyer outputs involve the mixer section of the Encoder Board.

- PROG VIDEO 1 and PROG VIDEO 2 are the outputs of the SCRIBE keyer. These outputs will show SCRIBE characters keyed over PROGRAM IN. INSERT ON/OFF and FADE controls the keying process.

  A bypass relay will route PROGRAM IN to VIDEO1 in the case of a power failure.

- PREV VIDEO is similar to PROG VIDEO 1 and PROG VIDEO 2 except that SCRIBE is always keyed over PROGRAM, regardless of INSERT conditions.

1.8.2.3 Prompts. The PROMPTS output displays commands and user information (such as font specifications, current operating modes, and system prompts) for use while operating the SCRIBE system. This output should be connected to a separate black & white monitor during operation.

1.8.2.4 Other Outputs. These outputs include the optional PREVIEW and RGB component video outputs.

- PREVIEW is used for optional separate output preview channel, providing non-antialiased SCRIBE text and backgrounds.

- RED provides "RED" component output in systems fitted with the RGB component video option.

- GREEN provides "GREEN" component output in systems fitted with the RGB component video option. Also, the component SYNC signal is mixed into the GREEN output.

- BLUE provides "BLUE" output in systems fitted with the RGB component video option.

- KEY provides a key signal, timed to the RGB component video option outputs.

Refer to Figure 1-2 (SCRIBE Hook-Up Diagram) for more information.

1.9 SCRIBE PHYSICAL INSTALLATION

1.9.1 MAINFRAME

The SCRIBE mainframe is designed for rack-mount installation. The mainframe must be securely mounted in a standard 19" equipment rack. The mounting location must have adequate ventilation, and the location must be free of vibration. The SCRIBE mainframe is powered by 115 VAC/60 Hz and requires .8A. (optional: 230 VAC/50 Hz, 4A) Refer to Figure 1-1, SCRIBE Mainframe, Rear Panel.

1.9.2 KEYBOARD

The keyboard console is a table-top device that connects to the mainframe through a four-wire cable with locking connectors. The keyboard may be remoted up to 1000 feet away from the mainframe, and additional keyboards may be added to the system if necessary. Each keyboard contains its own power supply, and is powered by 115 VAC/60 Hz, 1A (optional: 230 VAC/50 Hz, 0.5A).

1.9.3 GPI CONNECTIONS

The GPI (General-Purpose Interface) connector allows you to externally control SCRIBE functions that are stored under Function Keys F9 and F10 (for more information about the Function Keys, refer to SCRIBE Operation Manual, Publication No. 2A0-0979, Part III, paragraph 2.5.20).

1.9.3.1 **GPI Operation.** The required connector for the GPI is supplied with the SCRIBE system. When GPI pins 1 and 2 are connected (using a pushbutton, relay closure, etc.), the function stored under Function Key F9 is executed. When GPI pins 3 and 4 are connected, the function stored under Function Key F10 is executed.

A typical application for the GPI would be to store a read-next command under either F9 or F10. Then, a push-button switch would be used by a news commentator to perform read-nexts on cue. Since there is no limit to the possibilities of the Function Keys, there is no limit to the applications of the GPI function.

The only requirements of this function is that the switch or relay closure lasts for at least 80 ms, and that successive switch or relay closures are spaced at least 80 ms apart to allow for debouncing.

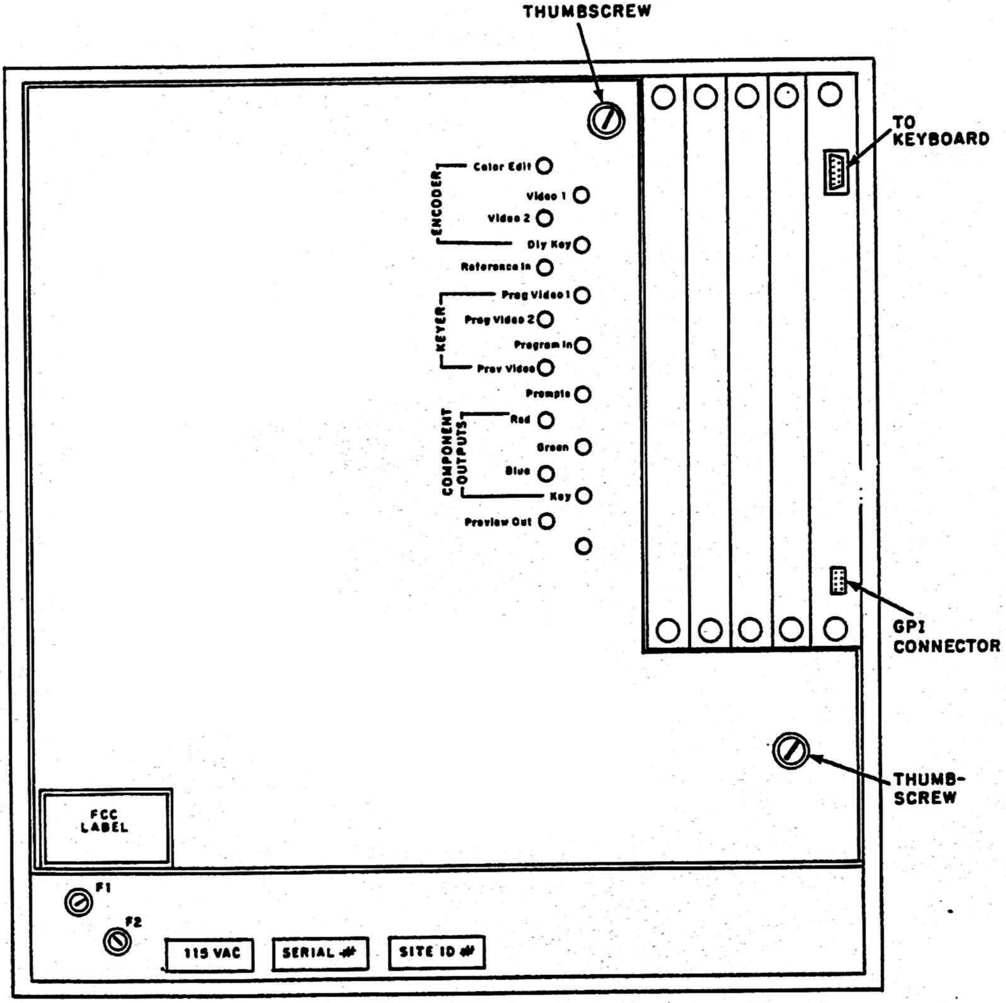
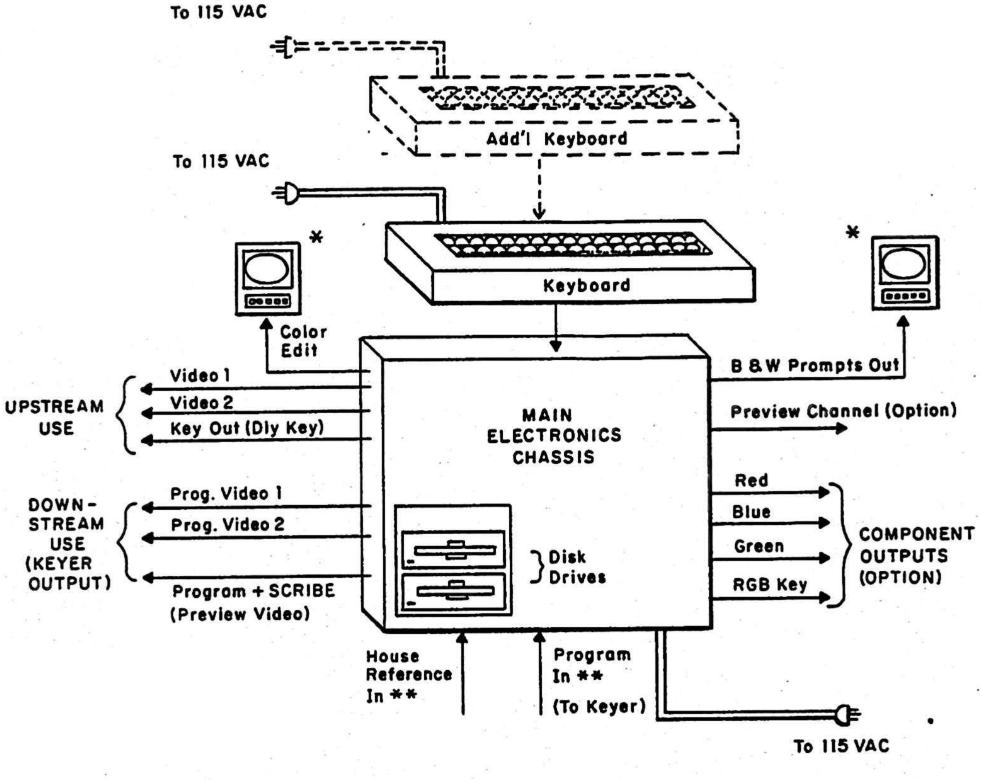

THUMBSCREW
TO KEYBOARD
ENCODER
Color Edit
Video 1
Video 2
Dly Key
Reference In
KEYER
Prog Video 1
Prog Video 2
Program In
Prev Video
Prompts
COMPONENT OUTPUTS
Red
Green
Blue
Key
Preview Out
GPI CONNECTOR
THUMB-SCREW
FCC LABEL
F1
F2
115 VAC
SERIAL #
SITE ID #

Figure 1-1. SCRIBE Mainframe, Rear Panel


To 115 VAC
Add'l Keyboard
To 115 VAC
*
Keyboard
*
Color
Edit
Video 1
Video 2
Key Out (Dly Key)
UPSTREAM
USE
MAIN
ELECTRONICS
CHASSIS
B & W Prompts Out
Preview Channel (Option)
DOWN-
STREAM
USE
(KEYER
OUTPUT)
Prog. Video 1
Prog. Video 2
Program + SCRIBE
(Preview Video)
Disk
Drives
Red
Blue
Green
RGB Key
COMPONENT
OUTPUTS
(OPTION)
House
Reference
In **
Program
In **
(To Keyer)
To 115 VAC

* Video Monitors Are Supplied By User
** Jumper option allows PROGRAM IN or REFERENCE IN to be used as reference source.

Figure 1-2. SCRIBE Hook-Up Diagram

1.10 SCRIBE SETUP AND ADJUSTMENTS

There are several video adjustments and configuration selections that are available to the user. The adjustments must be performed to ensure maximum video quality. The configuration selections involve selecting either REFERENCE IN or PROGRAM IN as the reference source for the SCRIBE. (As shipped, the SCRIBE uses PROGRAM IN as its reference source, and REFERENCE IN is not connected.)

1.10.1 REFERENCE SOURCE SELECTION

As shipped, the SCRIBE uses PROGRAM IN as its reference source. However, there are some applications that require the SCRIBE to use REFERENCE IN as the reference source, rather than PROGRAM IN.

In the PROGRAM IN reference configuration, J20 on the Encoder Board (REF VIDEO) is connected to P3 on the Analog Transition Board (see Figure 1-3 "A"). To use REFERENCE IN as the SCRIBE reference source, you must disconnect J20 and P3, and then connect the REFERENCE IN backplane connector to P3 (shown in Figure 1-3 "B").

The Encoder Board is located on the inside rear door of the SCRIBE chassis; the Analog Transition Board is located on the lower left of the backplane interconnection board. Both locations are shown in Figure 1-4.

To enable the SCRIBE to use REFERENCE IN:

1. Disconnect A.C. power to the SCRIBE.

2. Open the back door of the SCRIBE by turning the thumbscrews counterclockwise. Note the locations of the Encoder Board and the Analog Transition Board (refer to Figure 1-4).

3. Locate the green "Chabin" cable linking J20 on the Encoder Board with P3 on the Analog Transition Board. Disconnect this cable.

4. Using a 25-inch "Chabin" cable, connect the REFERENCE IN back panel connection to P3 on the Analog Transition Board.

5. Check the work area for any tools or other foreign material, then close the chassis rear door. Secure the door by rotating the thumbscrews clockwise.

6. Reconnect A.C. power.

The SCRIBE is now configured to use REFERENCE IN as its internal reference source.

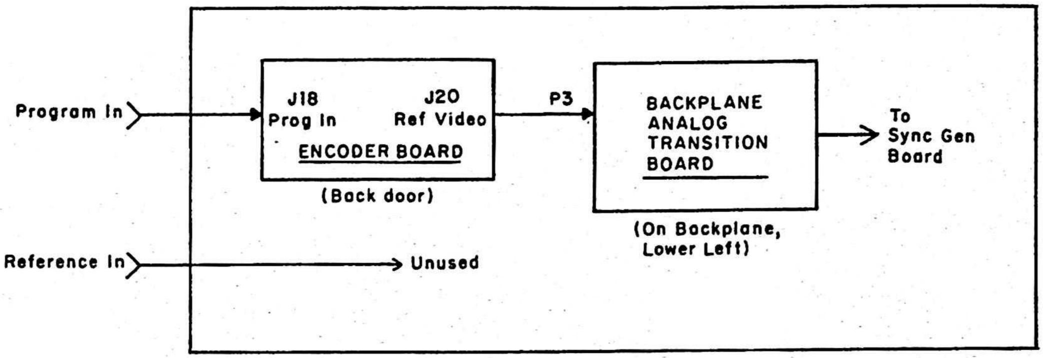

Program In
J18
Prog In
J20
Ref Video
ENCODER BOARD
(Back door)
P3
BACKPLANE
ANALOG
TRANSITION
BOARD
(On Backplane,
Lower Left)
To
Sync Gen
Board
Reference In
Unused

Figure 1-3 "A". Normal (Program In as reference) Operation

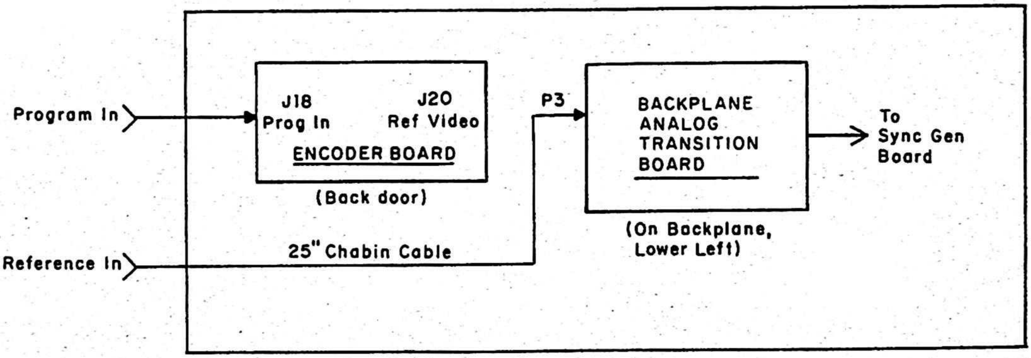

Program In
J18
Prog In
J20
Ref Video
ENCODER BOARD
(Back door)
P3
BACKPLANE
ANALOG
TRANSITION
BOARD
(On Backplane,
Lower Left)
To
Sync Gen
Board
Reference In
25" Chabin Cable

Figure 1-3 "B". Reference Input Operation

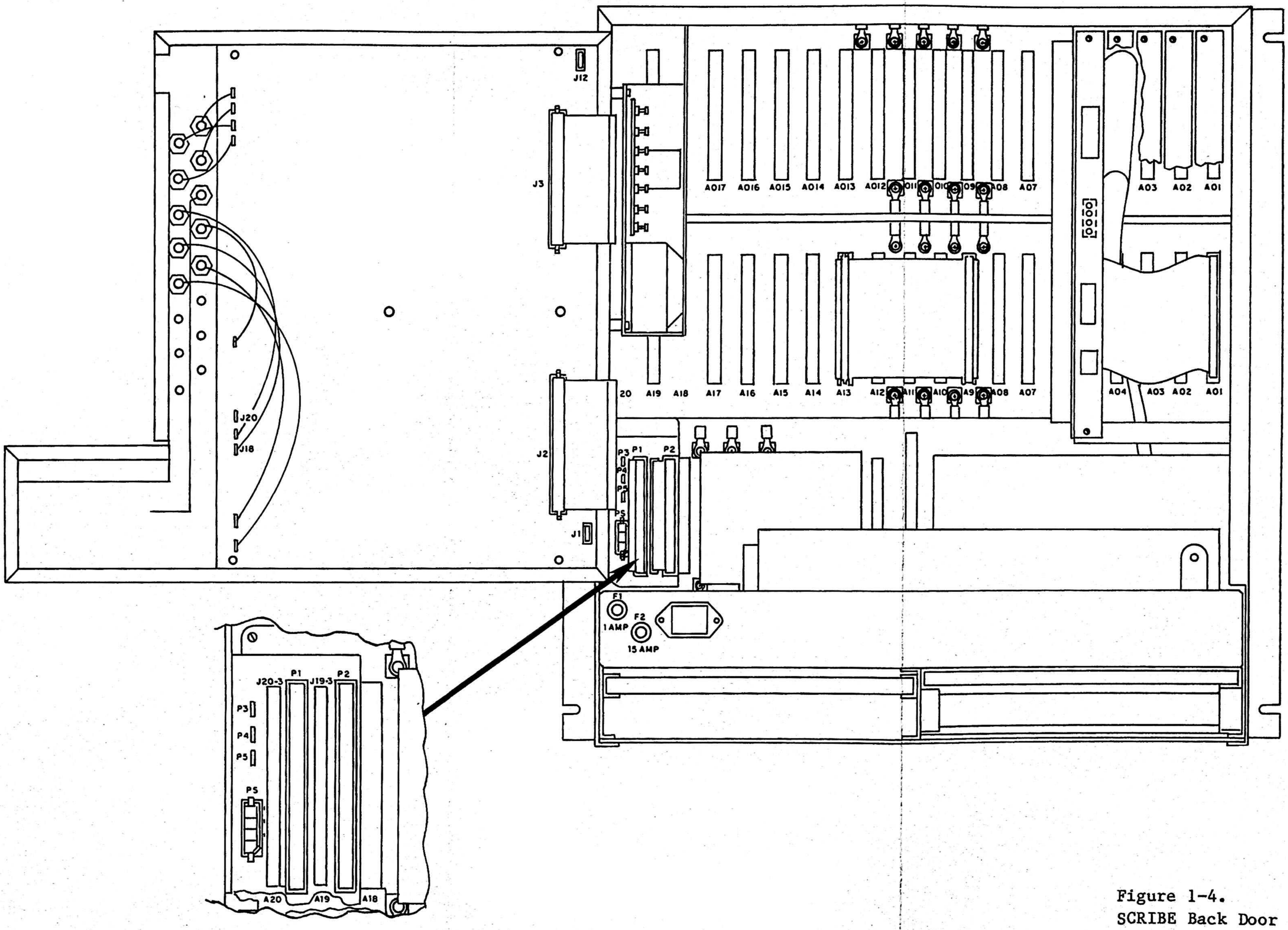

J12
J3
J2
J1
J20
J18
A017
A016
A015
A014
A013
A012
A011
A010
A09
A08
A07
A03
A02
A01
20
A19
A18
A17
A16
A15
A14
A13
A12
A11
A10
A9
A08
A07
A04
A03
A02
A01
P3
P1
P2
P4
P5
P5
F1
1 AMP
F2
15 AMP
J20-3
P1
J19-3
P2
P3
P4
P5
P5
A20
A19
A18

Figure 1-4.
SCRIBE Back Door
and Backplane

1.10.2 USER VIDEO ADJUSTMENTS

There are several video adjustments available to the user in order to ensure maximum video quality. These adjustments are located on the front panel of the Sync Generator Board, which can be reached by opening the SCRIBE front panel. Refer to Figure 1-5 for the locations of these adjustments.

1.10.2.1 **R6, CHROMA FREQUENCY.** R6 adjusts the frequency of the chroma subcarrier when the system is operating stand-alone.

1.10.2.2 **R7, H-PHASE.** R7 adjusts H-phase in respect to the subcarrier of the signal while in stand-alone, and can be used to calibrate the SCRIBE to RS-170A.

When the SCRIBE is genlocked to an external video signal, R7 adjusts the H-phase of the SCRIBE to the H-phase of the incoming video.

1.10.2.3 **R15, FINE CHROMA PHASE.** R15 is used to for fine adjustment of chroma phase of SCRIBE video with respect to the genlock source.

1.10.2.4 **R20, VERTICAL PHASE.** R20 is used to adjust the phase of the SCRIBE to the V-phase of the incoming video signal.

1.10.2.5 **R21, BURST POSITION.** R21 is used to adjust the position of the burst phase with respect to picture blanking start/end.

1.10.2.6 **R22, BURST WIDTH.** R22 adjusts the duration of the burst signal, which should be nine cycles of SC from +20 IRE to -20 IRE.

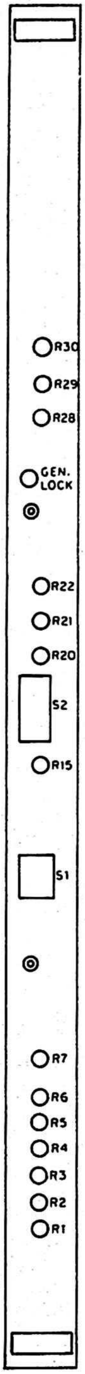

R30
R29
R28
GEN. LOCK
R22
R21
R20
S2
R15
S1
R7
R6
R5
R4
R3
R2
R1

Figure 1-5. Sync Generator Board, Adjustment Locations

1.10.2.7 S1 - 1, WHITE ENABLE. S1 is a four-bank DIP switch, in which switch #1 is used for white enable. When S1 - 1 is on, it sets white level at 100 IRE. When off, this switch sets white level at 77 IRE. The SCRIBE is shipped with S1 - 1 in the off position.

1.10.2.8 S1 - 2, LUMA NOTCH DISABLE. S1 - 2 is used to enable or disable the SCRIBE luminance notch filter. When on, this switch disables the luma notch filter. When this switch is off, the luma notch filter is enabled. The SCRIBE is shipped with S1 - 2 in the off position.

1.10.2.9 S1 - 3, CHROMA DISABLE. S1 - 3 is used to enable or disable subcarrier so that the SCRIBE displays either monochrome or color. When S1 - 3 is in the on position, subcarrier is disabled, and the SCRIBE displays monochrome only. When this switch is in the off position, subcarrier is enabled and the SCRIBE is in full color operation. The SCRIBE is shipped with S1 - 3 in the off position.

1.10.2.10 S1 - 4. S1 - 4 is not currently used.

1.10.2.11 S2, COARSE CHROMA PHASE. S2 is a 10-position rotary switch used for coarse adjustment of the chroma phase of SCRIBE-generated video with respect to the genlock source.

1.10.2.12 J5 (on Encoder board), SYNC TIMING. J5 is a nine-position jumper located on the Encoder board (located on the inside rear door of the SCRIBE). J5 is used to move the position of sync in relation to blanking.

1.11 ADDITIONAL STORAGE SYSTEMS

1.11.1 GENERAL

Instructions for installing additional storage systems (floppy disk drives, hard disk drives, tape drives, controllers) are supplied with the equipment. However, additional storage systems require that the system's Drive Configuration Table be modified after installation. This procedure involves entering specification values for each additional storage system into the table. Complete instructions for this procedure appear below.

1.11.2 MODIFYING DRIVE CONFIGURATION TABLE

The SCRIBE Drive Configuration Table is a Disk Utility Program function that allows you to add or remove disk drives or controllers to or from the system. The Configuration Table contains 20 specification values, which specify the type of drive and its format.

The values for the drive specification are supplied with the disk drive to be installed. These values are entered into a menu format, which is then recorded on your start-up disk.

Follow this procedure to modify the Table:

Step 1: From the SCRIBE Operating System Loading Menu (Figure 1-6), select Disk Utilities by entering "D". The system will display the Disk Utility Menu, Figure 1-7.

```
CHYRON SCRIBE OPERATING SYSTEM 1.00

D.........DISK UTILITY
M.........MESSAGE COMPOSE
F.........FONT CREATE UTILITY
B.........REBOOT SYSTEM
R.........RESTART SYSTEM
```

Figure 1-6. Operating System Loading Menu

```
SCRIBE DISK UTILITY FUNCTIONS

[1]      COPY
[2]      RENAME
[3]      DELETE
[4]      DISPLAY
[5]      MODIFY DRIVE CONFIGURATION TABLE
[6]      FORMAT & INITIALIZE

SELECT FUNCTION [1-6]
```

Figure 1-7. Disk Utility Menu

NOTE

Copy the configuration table onto a floppy disk using the "COPY" function before modifying the configuration table on your boot-up disk. This will prevent you from damaging the configuration table on your boot-up disk by mistake. When the table has been modified properly and has been tested, copy the table onto your boot-up disk.

Step 2: Select the Modify Drive Configuration Table function by entering "5". The system will respond with Figure 1-8.

```
5.     MODIFY DRIVE CONFIGURATION TABLE

       From Drive:
```

Figure 1-8. Modify Drive Configuration Menu

Step 3: Enter the ID of the drive containing the disk with the current version of the Configuration Table. Thus, if the disk you're working with is in Drive #2, enter "2" here. The system will display a list of the storage systems from the Configuration Table, as shown in Figure 1-9.

```
5.     MODIFY DRIVE CONFIGURATION TABLE

Drive:   2.  HARD
         3.  FLOPPY
         4.  FLOPPY
         5.
         6.
         7.
         8.
         9.

Enter Drive ID to be modified -
NEWLINE records table
```

Figure 1-9. Drive Listing

Step 4: Now, enter the Drive ID to be modified. This means if you are adding a drive the the system, which you want to call Drive #5, enter "5" here.

(This works the same if you are removing a drive, or if you want to change a drive ID from one type of drive to another. If, for example, you want to change Drive #3, a floppy drive, to a hard disk drive, you would enter "3" here, then go about installing a hard drive. Also, drives need not be installed consecutively. Thus, you could have drives at ID numbers 2, 4, 7, and 9 if you wished.)

The system will now display the Drive Configuration Table for the selected Drive ID number (Figure 1-10).

```
                 DRIVE CONFIGURATION TABLE

 FROM DRIVE 2:                 DRIVE ID:  5
(location of the table)        (drive ID being
                                modified)


 [1] CONTROLLER:               [11]  P TABLE 0:
 [2] PHYSICAL LUN:             [12]          1:
 [3] DEVICE TYPE:              [13]          2:
 [4] SECTORS PER BLOCK:        [14]          3:
 [5] SECTORS PER TRACK:        [15]          4:
 [6] TIMEOUT VALUE:            [16]          5:
 [7] MAXIMUM BLOCK ADDR:       [17]          6:
 [8] READ AFTER WRITE:         [18]          7:
 [9] FORMAT INTERLEAVE:        [19]          8:
 [10] HEAD PARKING ZONE:       [20]          9:

  ENTER ALL VALUES - PRESS NEWLINE TO ENTER
```

Figure 1-10. Drive Configuration Table Display

Step 5: From the Drive Configuration specification sheet supplied with the drive, enter the specified values into Items [2] through [7], and Items [9] through [20]. Items [1], [2], and [8] are specific to the system installation, and will be covered in Steps 9 through 9.

Step 6: The CONTROLLER ID: field value [1] depends on the number of disk controllers in use in the system. This depends, in turn, on how the ID jumper is placed on the controller(s), since multiple controllers are connected through a daisy-chain interface. Up to seven controllers can be used with the SCRIBE, so the Drive Configuration Table must specify which controller is to be used for the added drive. **NOTE:** Controllers 1 through 7 are reserved for disk drives. Controller 8 is reserved for tape drive systems.

Table 1-1. CONTROLLER ID: Values

# of Controllers In System	CONTROLLER ID:
1 Controller	1
2 Controllers	2
3 Controllers	4
4 Controllers	8
5 Controllers	16
6 Controllers	32
7 Controllers	64

Step 7: Enter the proper CONTROLLER ID: value for your configuration into Item [1] on the Drive Configuration Table menu.

Step 8: The PHYSICAL LUN (Logical Unit Number): value [2] is dependent on how the installed drive is to be addressed by the controller to which it is attached..

Note that the PHYSICAL LUN is different that the Drive ID. The Drive ID is how the operator calls the drive during operation of the system, while the PHYSICAL LUN is how the drive is addressed by its controller (LUN on a drive is set in the hardware by a jumper on the drive unit).

The internal Disk Controller board of the SCRIBE has four available sites to install drives. Of these, two sites are reserved for hard disks and two sites are reserved for floppy disks. The two hard disk sites are addressed as PHYSICAL LUN 0 and 1. The two floppy disk sites are addressed as PHYSICAL LUN 2 and 3. Thus, in the basic SCRIBE, the one hard disk drive occupies PHYSICAL LUN:0 and the one floppy disk drive occupies PHYSICAL LUN:2. If you were to add a floppy disk drive, it would be addressed by the controller as PHYSICAL LUN:3.

Determine the LUN: of the installed device. Enter the value into the Drive Configuration Table menu.

Step 9: The READ AFTER WRITE: (Item [8]) field allows you to specify whether or not the installed device will provide error checking.

"READ AFTER WRITE" error checking causes the SCRIBE to verify each device write with a read. If an write error is detected, it is posted and recorded in the Disk Error Log.

Occasionally, error checking is not desirable since with error checking, device operation is somewhat slower. CHYRON recommends that you use this error checking subroutine if possible.

To enable read-after-write error checking, set the READ AFTER WRITE: field to 1. To disable read-after-write error checking, enter 0 in this field.

Step 10: The Drive Configuration Table menu should be completely filled out by this point. (If you wish to erase all the fields and re-enter them, press the ERASE key.) Press NEWLINE to record the entry.

NOTE

When you add an entry to the Drive Configuration Table, you must re-boot the system using a boot-up disk containing the modified Drive Configuration Table in order for the system to recognize the changes.

Step 11: CHYRON recommends that you keep copies of the Drive Configuration Table. Use the Disk Utility COPY program to make backup copies in case of disk failure. NOTE: You must keep the current Configuration Table stored on your start-up disk. If you use the hard disk as your start-up disk, you must store a current configuration table there.

Section 2

SCRIBE SYSTEM OVERVIEW

2.1 INTRODUCTION

This section provides a complete of overview of the SCRIBE system, including overall physical setup, functional descriptions, and block diagrams of major subassemblies.

Also contained in this section is the procedure for how to read and interpret the operational error log and the boot-prom error codes. Therefore, study these procedures when initially diagnosing a system failure.

2.2 SCRIBE SETUP

The SCRIBE system follows a dual-microprocessor architecture, and is configured as shown in Figure 2-1. The system may be described in terms of major subsystems, which correspond to P.C. boards or groups of P.C. boards within the system. These subsystems are as follows:

- Keyboard
- Transition Board
- MVME117 CPU Board
- Disk Controller/Disk Systems
- Dual Ported Memory
- BMPU (bit-slice) processor
- Frame Buffers
- Video Display Board
- Analog Video Board

The various subsystems are connected through a backplane arrangement. All intra-system communications are accomplished through two standard VMX buses and one VME bus.

All subsystems for the SCRIBE are contained in a single card-cage chassis, and are connected through several backplane boards. The chassis physical setup is shown in Figure 2-2.

2.3 HARDWARE OVERVIEW

2.3.1 KEYBOARD

The SCRIBE keyboard is the device used for entering text and control information into the system. The keyboard sends serialized data to the MVME117 CPU board through the transition board. The MVME117 CPU board echoes address data back to the Address Readout LEDs on the keyboard.

2.3.2 CPU TRANSITION BOARD

The CPU Transition Board subsystem consists of a P.C. board interfaced with the keyboard subsystem and the MVME117 CPU board. The transition board converts serialized data from the keyboard (RS422) to RS232 serial data for the MVME117 CPU. Also located on the CPU transition board are the SCSI bus terminators and the GPI triggering logic.

The SCSI specification requires the SCSI bus to be terminated at both ends. The bus is terminated on this board, and on the disk controller board, to satisfy this requirement.

There are two GPI inputs to the CPU Transition Board. These inputs go to Schmitt-trigger devices, which in turn are connected to the modem control lines of the MVME117 CPU Board. On the MVME117 Board, the U/ART device posts interrupts to the CPU depending on which set of GPI contacts were closed.

These interrupts trigger specific actions in the SCRIBE: closing pins 1 and 2 causes the function stored under function key F9 to be executed, closing pins 3 and 4 causes the function stored under function key F10 to be executed.

For more information about the GPI, refer to Section 1, paragraph 1.8.4 of this manual.

2.3.3 MVME117 CPU BOARD

The MVME117 CPU board is a one-board microcomputer based on the Motorola 68010 CPU. The MVME117 board communicates with virutally every other system component, and is the VMEbus system controller and bus master.

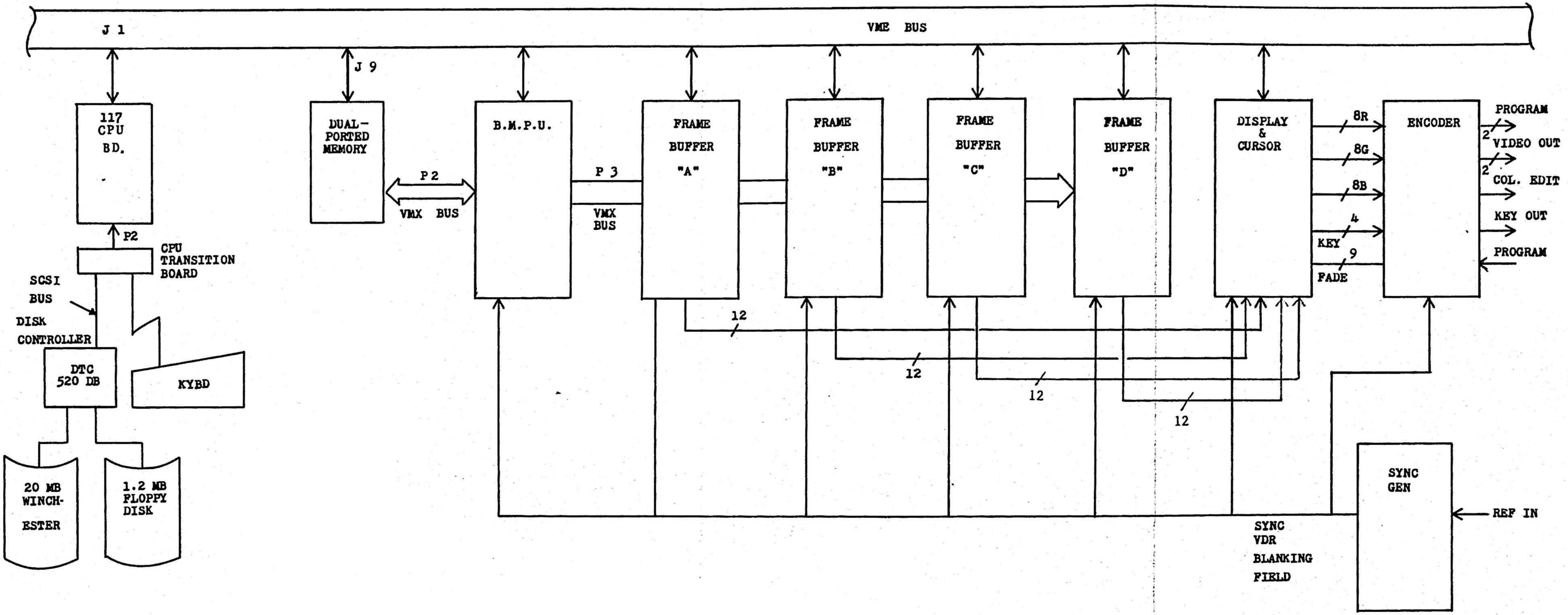

J 1
VME BUS
J 9
117 CPU BD.
P2
CPU TRANSITION BOARD
SCSI BUS
DISK CONTROLLER
DTC 520 DB
KYBD
20 MB WINCH-ESTER
1.2 MB FLOPPY DISK
DUAL-PORTED MEMORY
P 2
VMX BUS
B.M.P.U.
P 3
VMX BUS
FRAME BUFFER "A"
FRAME BUFFER "B"
FRAME BUFFER "C"
FRAME BUFFER "D"
12
12
12
12
DISPLAY & CURSOR
8R
8G
8B
4
KEY
9
FADE
ENCODER
2
2
PROGRAM VIDEO OUT
COL. EDIT
KEY OUT
PROGRAM
SYNC GEN
REF IN
SYNC
VDR
BLANKING
FIELD

Figure 2-1. SCRIBE Overall Block Diagram. 2-3/2-4

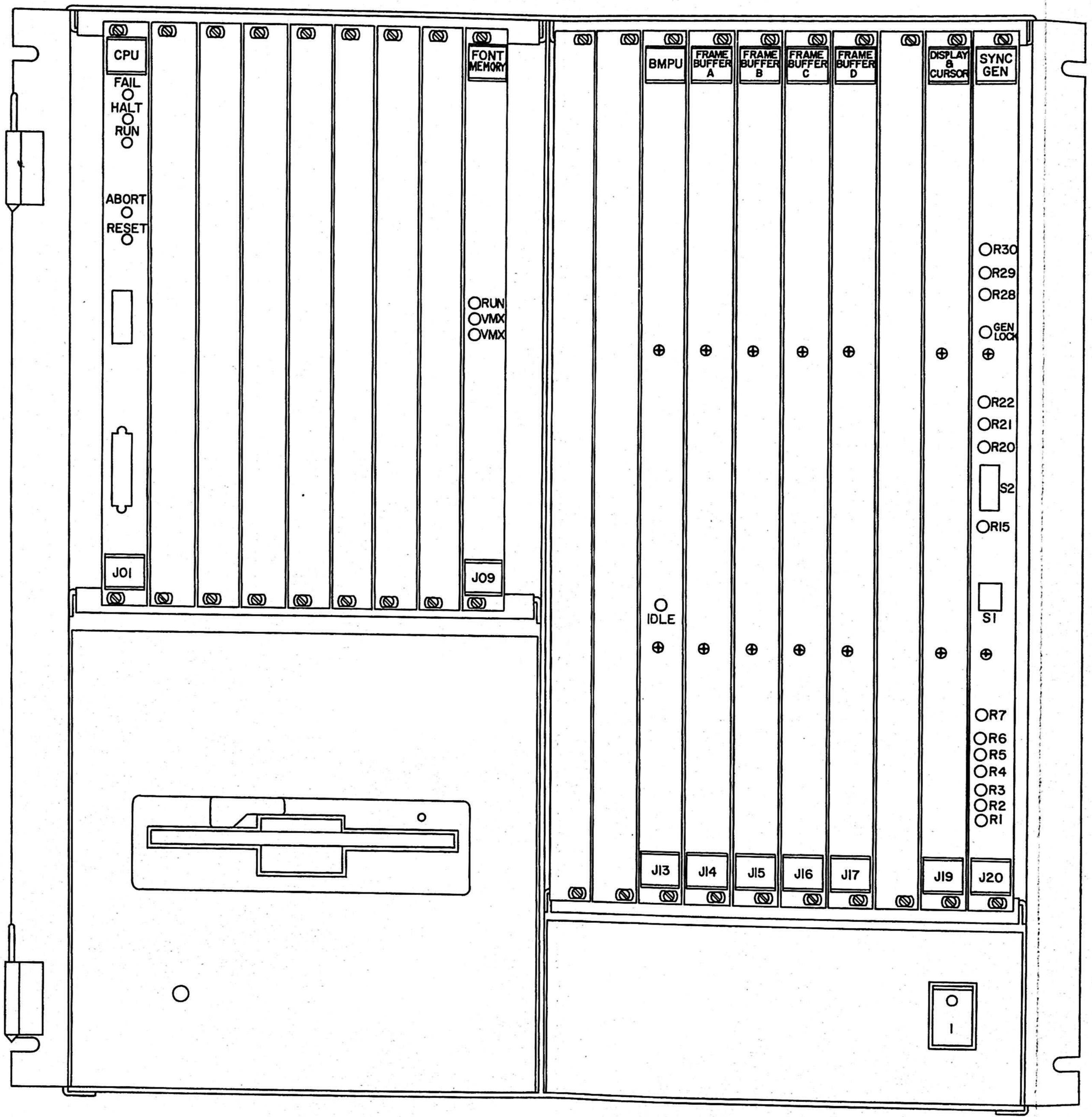

CPU
FAIL
HALT
RUN
ABORT
RESET
J01
FONT MEMORY
RUN
VMX
VMX
J09
BMPU
FRAME BUFFER A
FRAME BUFFER B
FRAME BUFFER C
FRAME BUFFER D
DISPLAY & CURSOR
SYNC GEN
R30
R29
R28
GEN LOCK
R22
R21
R20
S2
R15
S1
IDLE
R7
R6
R5
R4
R3
R2
R1
J13
J14
J15
J16
J17
J19
J20

Figure 2-2. SCRIBE Chassis Front Physical Setup

The MVME117 board carries 512K bytes of RAM, RS232 serial port, a SCSI (small computer, standard interface) host interface adapter, and optional floating-point coprocessor, and a VMEbus interface with system controller functions.

The MVME117 CPU Board is not directly used as a graphics processor. The CPU indirectly controls the actual graphics processor (the BMPU or Bit-Slice subsystem) through commands and data over the VME bus. Also, the CPU controls all peripheral devices, including font memory, the frame buffers, and the disk controller.

A complete diagnostic program is in place for this subsystem. Also, several components on this board are self-tested during power-up.

2.3.4 DISK CONTROLLER/DISK DRIVES

The disk controller and disk drives enable the user to store and recall displays, font data, programs, microcode, and related information. The disk controller is a DTC 520 DB microprocessor-based device with on-board data separation logic. The controller can handle 5.25-inch Winchester hard disk drives and multiple floppy-disk drives. The disk controller consists of a single-sided P.C. board, measuring 5.75 inches by 8.0 inches.

The SCRIBE system is shipped with one Seagate ST225 hard disk drive with 20M bytes of storage, and one Panasonic JU-475-2 floppy disk drive with 1.2M bytes of storage. Additional drives may be added to the system as needed.

2.3.5 DUAL PORTED MEMORY

The Dual Ported Memory board (font memory) is used to store font and display list data. The board contains up to 2M bytes of dual-ported RAM, and this memory space can be used by either the VME bus or the VMX bus.

The memory board generates odd parity for each byte written to RAM, and checks this parity bit during each read cycle. If a parity error is detected, the board interrupts the MVME117 on the VME bus. If such an interrupt occurs, the CPU reads the font memory status register to locate the error.

2.3.6 BIT SLICE PROCESSOR (BMPU)

The Bit Slice processor is the graphics controller for the SCRIBE system. The board communicates with the MVME117 CPU via the VME bus, and communicates with both the Font Memory and the Frame Buffers via two separate VMX buses. The hardware design is based on the AM29116 ALU and the AM2910A microsequencer controller. The board has 4K x 64 of microcode, in the form of RAM writeable control store (WCS).

2.3.7 FRAME BUFFERS

The frame buffers contain the pixel memory for the SCRIBE system. There are three interfaces to the memory: these are the VME bus, the VMX bus, and display control. The VME interface allows data to be written to or read from the memory via the VMEbus specification. The VMX interface allows data to be written to the memory according to the VMXbus specification. The display control generates the timing necessary to read the data from the memory into the serial shift registers and to clock the shift registers, which provides pixel data to the display board. The frame buffers reside on four P.C. board cards in the SCRIBE chassis.

2.3.8 DISPLAY BOARD

The display board receives the color look-up table index data from the Frame buffers, mixes the colors of the foreground and background look-up tagle addresses, then combines this data with the background color data. Both the Background and Character palettes are loaded into the display board through the VME bus.

The display board also contains the CRT controller for the diagnostic and operating prompts as well as the cursor controller. The cursor includes the tabs and safe-title markers. Both the CRT and cursor controllers are controlled in turn by the VME bus.

2.3.9 ANALOG VIDEO SECTION: SYNC GENERATOR, ENCODER

The SCRIBE video processing section is divided into a sync generator/genlock board and an encoder board. Together, these sections perform the task of converting the SCRIBE digital information plus the customer's input video and control signals into viable anti-aliased characters either stand-alone or over the customer's program video.

2.3.9.1 Sync Generator/Gen-Lock. The sync generator/genlock board is located in Slot 20 of the SCRIBE mainframe card cage, and operates as a gen-lockable sync generator which provides timing pulses to the digital control circuitry as well as the necessary encoding signals to the video encoder section.

The bit-clock will be dependent on the number of scan-line in the system (525 lines for NTSC version, 625 for PAL version) The following assumptions have been made to preserve the 4:3 aspect ratio of the display and to keep the pixels square.

For 525-line systems:

1) 772 bit clocks for each horizontal line interval
2) 640 pixels will be displayed (52.688 us)
3) 132 pixels will be blanked (10.870 us)
4) 58 clocks are horizontal sync interval (4.7 ± 0.1 us)
   480 scanlines will be displayed

For 625-line systems:

1) 940 bit clocks for each horizontal line interval
2) 762 pixels will be displayed (51.88 us)
3) 178 clocks will be blanked (12.12 us)
4) 70 clocks are horizontal sync interval (4.75 us)
5) 34 clocks will be EQ pulse width (2.45 us)
6) 575 scanlines will be displayed

When gen-locking to a video input, horizontal sync will lock to the input sync and subcarrier used for modulation will be locked to the burst gate signal of the composite video input. If no input is present, the subcarrier and the horizontal sync VCOs will free run to provide encoding signals.

When no gen-lock input is present, the horizontal and chroma VCOs will lock to each other by the following relationship:

$F_{sc} = (455/2) * F_h$ in the NTSC system

$F_{sc} = (909/4) * F_h$ in the PAL-M system

$F_{sc} = (1135/4) * F_h$ in the PAL system

Note that the PAL subcarrier will not have a 25 Hz offset, in the non genlock case.

2.3.9.2 **Video Encoder.** The video encoder section consists of one P.C. board, located on the inside of the SCRIBE mainframe rear door. This section encodes RGB data from the digital logic into composite video. The encoder is able to produces colors accurate to within one degree of phase and one degree of amplitude when viewed on a vectorscope. The encoder is factory configurable for either NTSC or PAL formats.

A 4-bit digital key signal must also be converted to composite video. This key signal must undergo a time delay equal to the delay of encoding the digital RGB data into composite video. The four key bits are treated as an unsigned integer equal to the amplitude of the key signal. A zero for the key bits is equivalent to 0 IRE for the key amplitude, while a 15 for the key bits is equivalent to 100 IRE key amplitude.

One bit of cursor information will have to be added to the composite video signal to generate color edit.

2.3.9.3 Preview Output (Optional). The preview video output provides the operator with a low-cost output containing non-antialiased characters plus cursor. This preview output is for operator preview, composition, and positioning only, and is not to be used as a broadcast output.

2.3.9.4 Keyer/Fader. This circuitry is located on the encoder board.

With the keyer/fader circuitry, a customer is able to insert the SCRIBE video over the input video as a downstream keyer. The ratio of SCRIBE video to Program video depends on the level of the key signal. Zero IRE for key level means 100% program video, while 100 IRE for key level means 100% SCRIBE video.

2.3.9.5 Prompt Video. The Prompt Video output provides prompt and status information to a black and white monitor for operator use. Prompt Video is a one bit signal originating on the Display & Cursor board, which is combined with sync and blanking and then output by the Encoder board to the monitor.

2.4 ERROR LOGGING

The SCRIBE system automatically logs any errors that may occur during operation. The SCRIBE system error log is a record of up to 99 errors, including the date and time when the error occurred, the type of error, and the address at which the error happened. This error log is useful for observing intermittent failures, and enables the maintenance technician to have a complete record of the system's performance.

The SCRIBE error log consists of two separate logs:

- Disk Error Log
- Miscellaneous Error Log

2.4.1 DISK ERROR LOG PROMPTS

The disk error log is a directory of up to 99 most recent failures (including both fatal and non-fatal errors) involving the disk storage subsystem.

Disk errors as they appear in the error log can be divided into two groupings:

- User Errors
- System Errors

2.4.1.1 **User Error Log Entries.** Disk errors that are caused by the user through improper operation are considered User Errors. User errors are almost always recoverable errors, which can be corrected by reselecting the proper drive, directory, etc. If a user error continues to occur, consult the SCRIBE Operation Handbook for more information.

A list of the disk error log (User Error) messages appears in Table 2-1, below.

Table 2-1. Disk Error Log: User Error Messages

04	DRIVE NOT READY
05	DRIVE NOT SELECTED
96	DISK NOT FORMATTED AND INITIALIZED
98	DRIVE ERROR - NO SPECIFICATION IN CONFIGURATION TABLE
99	DRIVE NOT SELECTED OR MOUNTED
9A	INVALID DRIVE ID
9B - 9F	[UNDEFINED]
A0	END OF DATA DETECTED
A5	ADDING TO NAME DIRECTORY AN ID & NAME THAT EXISTS
A6	FILE ID DOES NOT EXIST IN NAME DIRECTORY
A7	DRIVE ERROR - NO SPECIFICATION IN CONFIGURATION TABLE
A9 - B0	[UNDEFINED]
B1	CANNOT DELETE MESSAGE DIRECTORY ALREADY SELECTED
B2	MESSAGE DIRECTORY DOES NOT EXIST - CANNOT DELETE

Table 2-1. Disk Error Log: User Error Messages, continued

B3 - BA	[UNDEFINED]
BB	SYSTEM ID AND FILE ID MISMATCH - CANNOT USE DATA
BC - D8	[UNDEFINED]
DA - DE	[UNDEFINED]
DF	NO VALID DISK ADDRESS IN ROOT BLOCK DIRECTORY
E0	MESSAGE DIRECTORY NOT FOUND
E1	MESSAGE DIRECTORY ERROR
E2	DISK ERROR WHILE READING FILE TABLE
E3	[UNDEFINED]
E5	SHOW DIRECTORY ALREADY EXISTS - CANNOT CREATE
E6	DISK FULL - NO SPACE TO COMPLETE RECORD
E7	MESSAGE DIRECTORY FULL - CANNOT CREATE
E8	MAXIMUM NUMBER OF OPEN MESSAGE DIRECTORIES
EB	MAXIMUM NUMBER OF OPEN FILES EXCEEDED
EC	NO DIRECTORY FOUND FOR OPEN
ED	NO REFERENCE IN DIRECTORY FOR FILE BEING DELETED
F0	FILE ID ERROR
F3 - FF	[RESERVED FOR FUTURE USE]

2.4.1.2 System Error Log Entries. Disk errors that are caused by either the disk drives, the disk controller, or other system hardware and/or software and referred to as System Errors. System errors are not necessarily recoverable errors. System errors require maintenance in order to isolate the fault(s) involved. Base your diagnosis on type and frequency of system errors as recorded in the System Error Log. Possible courses of action include testing a suspect disk drive with a known good disk drive, checking disk controller connections, power supply levels, etc.

If required, run the Diagnostic Programs, which are described in Section 4 of this manual. If, through your courses of action you cannot restore proper system operation, please contact CHYRON Customer Service immediately.

A list of the disk error log (System Error) messages appears in Table 2-2.

Table 2-2. Disk Error Log: System Error Messages

81	SCSI BUSY WHEN TRYING TO ISSUE COMMAND
82	SCSI NO PHASE MATCH IN SELECTION PHASE
83	SCSI NO BUSY DETECTED AFTER CONTROLLER SELECTED
84	SCSI NO REQ BEFORE COMMAND PHASE
85	SCSI NOT IN COMAND PHASE
86	SCSI NOT IN COMMAND PHASE
87	SCSI PARITY ERROR DETECTED BY HOST
88	SCSI PHASE MISMATCH - SPURIOUS COMMAND PHASE DETECTED
89	SCSI UNDEFINED PHASE ERROR
8A	SCSI DATA OUT PHASE ERROR
8B	SCSI DATA IN PHASE ERROR
8C	SCSI STATUS PHASE ERROR
8D	SCSI CONTROLLER PARITY ERROR
8E	CONTROLLER ERROR CONDITION FROM SENSE BYTES
8F	SCSI MESSAGE IN PHASE ERROR
90	SCSI MESSAGE OUT PHASE ERROR
91	SCSI HOST PARITY ERROR DURING DATA OUT PHASE
92	SCSI HOST PARITY ERROR DURING DATA IN PHASE
93	ERROR WHILE READING SENSE BYTES
94	READ ERROR WHILE ATTEMPTING READ AFTER WRITE
95	READ AFTER WRITE DATA COMPARE ERROR
97	ILLEGAL SYSTEM FUNCTION CODE
A1	ATTEMPTING TO READ MESSAGE BUT DIRECTORY NOT OPEN
A2	ATTEMPTING TO RECORD DATA BUT DIRECTORY NOT OPEN
A3	DURING DELETE PREV BLK PTR DID NOT MATCH PREV BLK ADDR
A4	ADDING TO NAME DIRECTORY FILE ID THAT IS OUT OF RANGE
A8	DIRECTORY ID IS OUT OF RANGE
D9	DIRECTORY ADDRESS LOST FROM MEMORY

Table 2-2. Disk Error Log: System Error Messages, continued

E4	ATTEMPTING TO CLOSE UNOPENED MESSAGE DIR.
E9	ATTEMPTING TO READ FROM CLOSED FILE
EA	ATTEMPTING TO WRITE TO CLOSED FILE
EE	CLOSE ON UNOPENED FILE
EF	FILE NOT OPEN
F1	FILE ALREADY OPEN
F2	FILE OPEN - CANNOT BE DELETED
00	NO ERROR STATUS
01	NO INDEX SIGNAL
02	NO SEEK COMPLETE
03	WRITE FAULT
06	NO TRACK 0
07	MULTIPLE WINCHESTER DRIVES SELECTED
09	SEEK IN PROGRESS
0A - 0C	[RESERVED]
0D	SEEK IN PROGRESS
0E - 0F	[RESERVED]
10	TAPE EXCEPTION
11	UNCORRECTABLE DATA ERROR DURING READ
12	ID ADDRESS MARK NOT FOUND
13	DATA ADDRESS MARK NOT FOUND
14	RECORD NOT FOUND
15	SEEK ERROR
16	[RESERVED]
17	DRIVE WRITE PROTECTED
18	CORRECTABLE DATA FIELD ERROR
19	BAD BLOCK FOUND
1A	FORMAT ERROR
1B	[RESERVED]
1C	UNABLE TO READ ALTERNATE TRACK ADDRESS
1D	[RESERVED]
1E	ATTEMPTED TO DIRECTLY ACCESS ALTERNATE TRACK
1F	TAPE DRIVE FAILURE
20	INVALID COMMAND RECEIVED FROM HOST
21	ILLEGAL DISK ADDRESS
22	ILLEGAL FUNCTION FOR CURRENT DRIVE TYPE
23	VOLUME OVERFLOW
24 - 2F	[RESERVED]
30	RAM ERROR OR POWER UP SELF TEST ERROR
31	FDC 765 ERROR
32 - 3F	[RESERVED]

2.4.2 MISCELLANEOUS ERROR LOG

The miscellaneous error log is a directory of up to 99 most recent failures (including both fatal and non-fatal errors) involving SCRIBE systems other that the disk storage subsystem.

Miscellaneous errors as they appear in the error log can be divided into two groupings:

- User Errors
- System Errors

2.4.1.1 User Error Log Entries.

System errors that are caused by the user through improper operation are considered User Errors. User errors are almost always recoverable errors, which can be corrected by placing the (optional) printer on-line, loading paper into the printer, etc. Consult the SCRIBE Operation Handbook for more information.

A list of the system error log (User Error) messages appears in Table 2-3, below.

Table 2-3. Miscellaneous Error Log: User Error Messages

100	PRINTER NOT ATTACHED
101	PRINTER TIMEOUT
102	PRINTER OUT OF PAPER
103	PRINTER OUT OF PAPER
104	PRINTER OFF-LINE
105	PRINTER OPTION NOT IN SYSTEM

2.4.1.2 System Error Log Entries.

Miscellaneous errors that are caused by problems in the system hardware and/or software are referred to as System Errors. System errors are not necessarily recoverable errors, and as such, these errors require maintenance in order to isolate the fault(s) involved. Base your diagnosis on type and frequency of system errors as recorded in the error log. Many of these errors involve particular CPU addresses, which are listed in the prompt(s). Once an address is identified, consult the SCRIBE Memory Map (Table 2-5) in order to isolate the affected area. Possible courses of action include checking the boards for proper seating in the mainframe, looking for damaged boards/connections, checking power supply levels, etc.

If required, run the Diagnostic Programs, which are described in Section 4 of this manual.

If, through your courses of action you cannot restore proper system operation, please contact CHYRON Customer Service immediately.

A list of the Miscellaneous Error log (System Error) messages appears in Table 2-4:

Table 2-4. Miscellaneous Error Log: System Error Prompts

- PROGRAM EXECUTING
- BUS ERROR AT XXXXXXXX PC: XXXXXXXX SR:XXXX
- ADDRESS ERROR AT: XXXXXXXX PC: XXXXXXXX SR: XXXX
- ILLEGAL INSTRUCTION PC: XXXXXXXX SR: XXXX
- ZERO DIVIDE PC: XXXXXXXX SR: XXXX
- CHK INSTRUCTION PC: XXXXXXXX SR: XXXX
- TRAPV INSTRUCTION PC: XXXXXXXX SR: XXXX
- PRIVILEDGE VIOLATION PC: XXXXXXXX SR: XXXX
- TRACE PC: XXXXXXXX SR: XXXX
- 1010 EMULATOR PC: XXXXXXXX SR: XXXX
- 1111 EMULATOR PC: XXXXXXXX SR: XXXX
- UNASSIGNED PC: XXXXXXXX SR: XXXX
- FORMAT ERROR PC: XXXXXXXX SR: XXXX
- UNINITIALIZED INTERRUPT PC: XXXXXXXX SR: XXXX
- UNASSIGNED VECTOR PC: XXXXXXXX SR: XXXX
- AUTOVECTOR X ERROR PC: XXXXXXXX SR: XXXX
- UNEXPECTED INSTRUCTION TRAP PC: XXXXXXXX SR: XXXX
- UNEXPECTED INTERRUPT PC: XXXXXXXX SR: XXXX
- FONT MEMORY PARITY ERROR AT XXXXXXX BUS: XXX BANK: ...
- ....

2.4.3 DISPLAYING SYSTEM ERROR LOG

The system error log can be displayed through a Disk Utilities subroutine. Enter the Disk Utility program by selecting "D" from the SCRIBE Program Loading Menu. Then, select the "display" subroutine by entering "4". To display the System Error Log:

1. Enter "6" on the Display Menu when it appears on screen. Doing so displays the Error Log Menu (Figure 2-3).

```
4.  DISPLAY
6.  SYSTEM ERROR LOG DIRECTORY

[1] DISK ERROR LOG
[2] MISCELLANEOUS ERROR LOG

SELECT ERROR LOG TO BE DISPLAYED [1, 2]
```

Figure 2-3. Display Error Log Menu

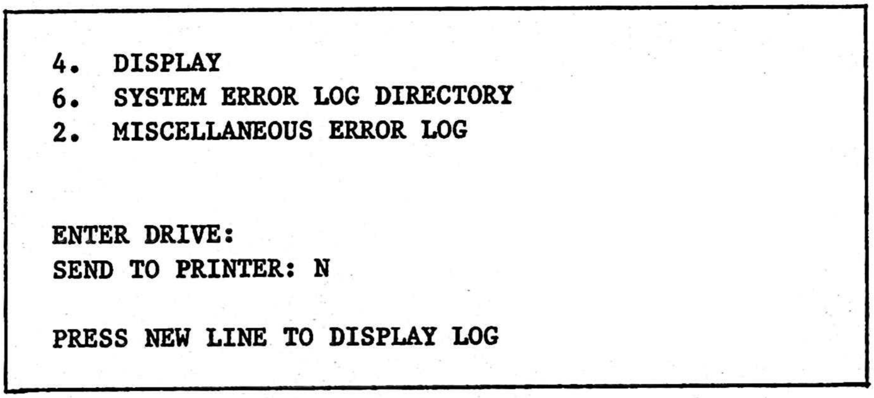
2. Enter either (1) or (2) to select the desired error log (Figure 2-4).

```
4.  DISPLAY
6.  SYSTEM ERROR LOG DIRECTORY
1.  DISK ERROR LOG


ENTER DRIVE:
SEND TO PRINTER: N

PRESS NEW LINE TO DISPLAY LOG
```

Figure 2-4. Display Disk Error Log Menu

or

Enter "2", and the Display Miscellaneous Error Log Menu (Figure 2-5) appears.



```
4.  DISPLAY
6.  SYSTEM ERROR LOG DIRECTORY
2.  MISCELLANEOUS ERROR LOG


ENTER DRIVE:
SEND TO PRINTER: N

PRESS NEW LINE TO DISPLAY LOG
```

Figure 2-5. Display Miscellaneous Error Log Menu

3. Enter a number that corresponds to the drive containing the disk from which you want to read the data.

4. The cursor automatically moves down to the SEND TO PRINTER line.

5. Press the <CR> key and the type of errors you requested will be displayed.

2.5 BOOT PROM ERROR CODES

When the SCRIBE is powered up, the boot-up program (stored in the boot PROMs) tests locations on the Display & Cursor board for specific function. If all sections of the Display & Cursor board are functional, the system's self-test will flag the board as working, and will proceed to the next test.

If, however, any section of the Display & Cursor board does not pass the power-up test, then the SCRIBE will output a two-digit hex error code. When this code is decoded into binary, the set bits reflect the type and location of the error.

The format for the error code is as follows:

DISPLAY & CURSOR ERROR CODE = $XX

ERROR TYPE	BIT NUMBER							
	7	6	5	4	3	2	1	0
Palette Memory Error	n	n	n	n	n	n	n	1
CRT Select Error	n	n	n	n	n	n	1	n
Channel Select Fade Latch	n	n	n	n	n	1	n	n
Fade Control Error	n	n	n	n	1	n	n	n
Alt. Palette Memory Error	n	n	n	1	n	n	n	n
Bknd. Palette Memory Error	n	n	1	n	n	n	n	n
Safe Title Memory Error	n	1	n	n	n	n	n	n

n = Don't Care

For example, if the boot PROM test detects several errors in the Display & Cursor board, these are displayed as a hex code, which may appear as follows:

DISPLAY & CURSOR ERROR CODE = $5A

(binary) 0 1 0 1 1 0 1 0

bit 4 bit 1

bit 6 bit 3

This error code corresponds to:

CRT SELECT ERROR	(bit #1 is set)
FADE CONTROL ERROR	(bit #3 is set)
ALT. PALETTE MEMORY ERROR	(bit #4 is set)
SAFE TITLE MEMORY ERROR	(bit #6 is set)

If, during power up for operation, you encounter a Display & Cursor Error Code, decode it using the above table, then examine the suspect areas using the Display & Cursor Diagnostic programs described in Section 4, paragraph 4.2.

Section 3

SCRIBE DETAILED THEORY OF OPERATION

3.1 GENERAL

This section provides descriptions of how each SCRIBE subsystem operates, as a precursor to detailed troubleshooting procedures. Theory descriptions are based on block diagrams of the particular subsystem.

3.2 KEYBOARD SYSTEM

The keyboard used with the SCRIBE system is a microcontroller- based device with its own source of program code. Keystrokes cause the device to generate ASCII codes, which are transmitted to the CPU Transition board using the RS-422 protocol. Additional keyboards are supported through a daisy-chain configuration.

A 8031 one-chip microcontroller and a custom IC are used to scan the keyboard matrix. When a key strike is detected, the IC sends the keystroke's location (in X, Y format) to the controller. The controller reads the key/code ROM (stored with the program code) and generates the proper ASCII code for the keystroke. This code is converted from parallel into serial data in the controller's internal UART, and is transmitted to the CPU Transition board via an RS-422 transceiver.

The keyboard also generates and displays address data using its Address Keypad and Address LEDs, and supports 24 discrete LEDs which are used to indicate color and font selection, etc. Address data is entered using the keyboard matrix procedure described above. The controller then enables the 4-digit LED readout and displays the address. Also, the controller enables the various discrete LED lamps on the keyboard based on operator selections.

When the SCRIBE system must display or increment an address on the Address Readout, or change the active color or font selections, the necessary data is transmitted from the mainframe to the keyboard using the RS-422 protocol.

The SCRIBE supports additional keyboards using a daisy-chain configuration. A number of separate keyboards can be connected together, with the powered-on keyboard nearest to the mainframe having control. Therefore, loop-through relays are used to connect the keyboard input to the keyboard output when the keyboard is powered down.

A functional block diagram of the SCRIBE Keyboard subsystem appears in Figure 3-1.

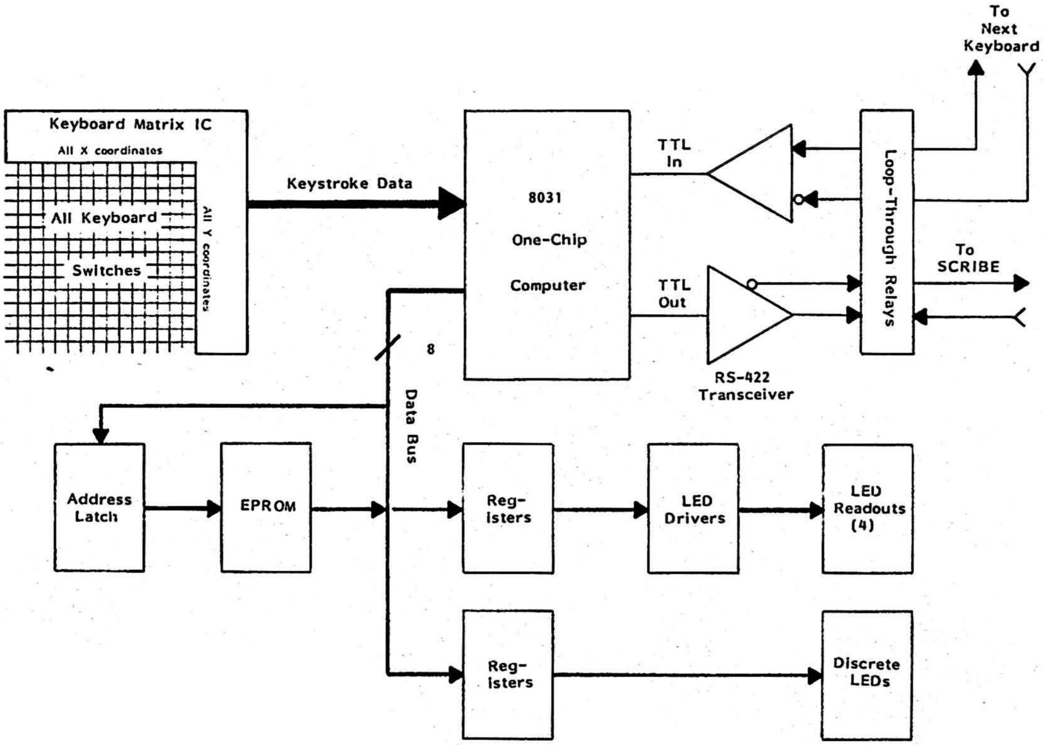

To Next Keyboard
Keyboard Matrix IC
All X coordinates
All Keyboard
Switches
All Y coordinates
Keystroke Data
8031
One-Chip
Computer
TTL In
TTL Out
Loop-Through Relays
To SCRIBE
RS-422 Transceiver
8
Data Bus
Address Latch
EPROM
Reg-isters
LED Drivers
LED Readouts (4)
Reg-isters
Discrete LEDs

Figure 3-1. SCRIBE Keyboard Functional Block Diagram

3.3 CPU TRANSITION BOARD

The CPU Transition board supports communication between the keyboard and the CPU board. Since the keyboard-to-transition interface uses the RS-422 specification, and the transition-to-CPU interface uses the RS-232 specification, an intermediate two-way conversion is necessary. The transition board is used to convert the RS-422 serial keyboard data output into RS-232 serial data for the CPU board. A block diagram of the transition board appears in Figure 3-2.

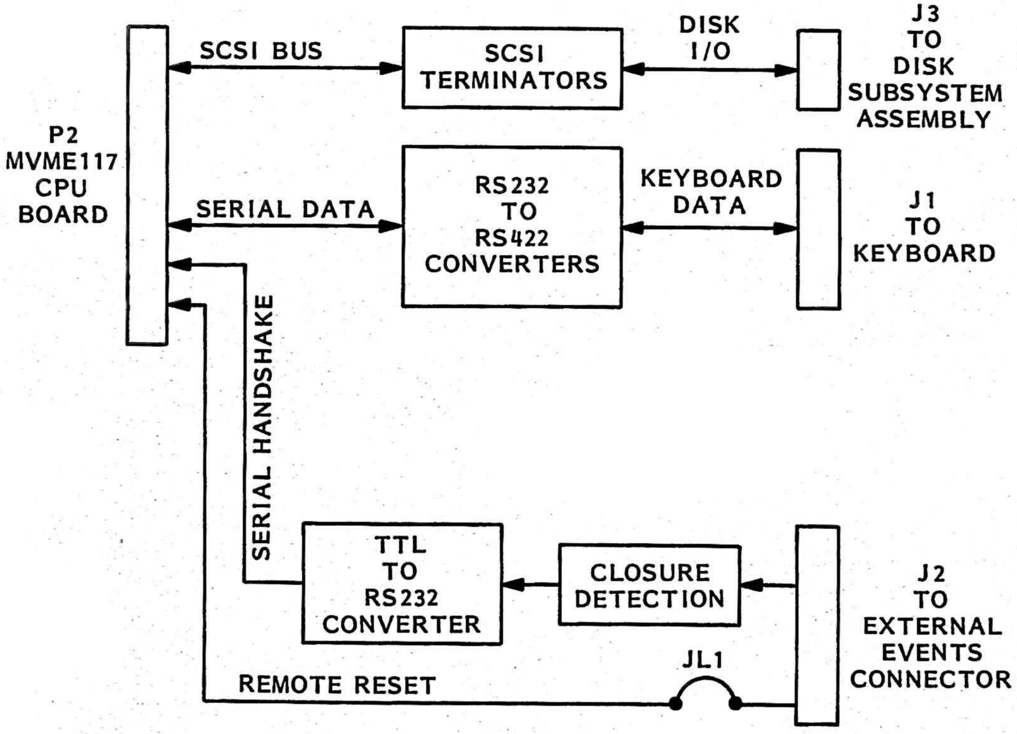

P2
MVME117
CPU
BOARD
SCSI BUS
SCSI
TERMINATORS
DISK
I/O
J3
TO
DISK
SUBSYSTEM
ASSEMBLY
SERIAL DATA
RS232
TO
RS422
CONVERTERS
KEYBOARD
DATA
J1
TO
KEYBOARD
SERIAL HANDSHAKE
TTL
TO
RS232
CONVERTER
CLOSURE
DETECTION
J2
TO
EXTERNAL
EVENTS
CONNECTOR
JL1
REMOTE RESET

Figure 3-2. CPU Transition Board Functional Block Diagram

Troubleshooting for the transition board involves testing with an oscilloscope to determine if signals are being properly sent from the CPU to the transition board, and then testing if signals are being passed from the keyboard to the transition board. Any signal garbling that may be occurring in this subsystem will become apparent after these tests. Diagnostics for this board are contained in the Diagnostic Program, which is documented in Section IV of this manual.

3.4 MVME117 CPU BOARD

The MVME117 CPU board is the master controller of all functions within the SCRIBE system. The board supports the VMEbus specification as bus master, and has an on-board RS-232 interface, a RESET pushbutton, an ABORT pushbutton, and an eight-bank DIP configuration switch. An optional floating-point co-processor is available; this speeds certain arithmetic functions of the CPU board. The board is constructed using a two-layer physical architecture, and is contained on one half-height Eurocard plug-in board. A detailed block diagram of the CPU board appears in Figure 3-3.

3.4.1 CPU

The CPU board is based on the MC68010 microprocessor, which is used as the system's master controller. The MC68010 is a 16-bit processor with 32-bit internal registers, and supports up to 16 megabytes of virtual memory. Timing for the CPU and its associated circuitry operates at 10 MHz, and is derived from a 40 MHz oscillator. The MC68010 is contained in a 64-pin DIP package.

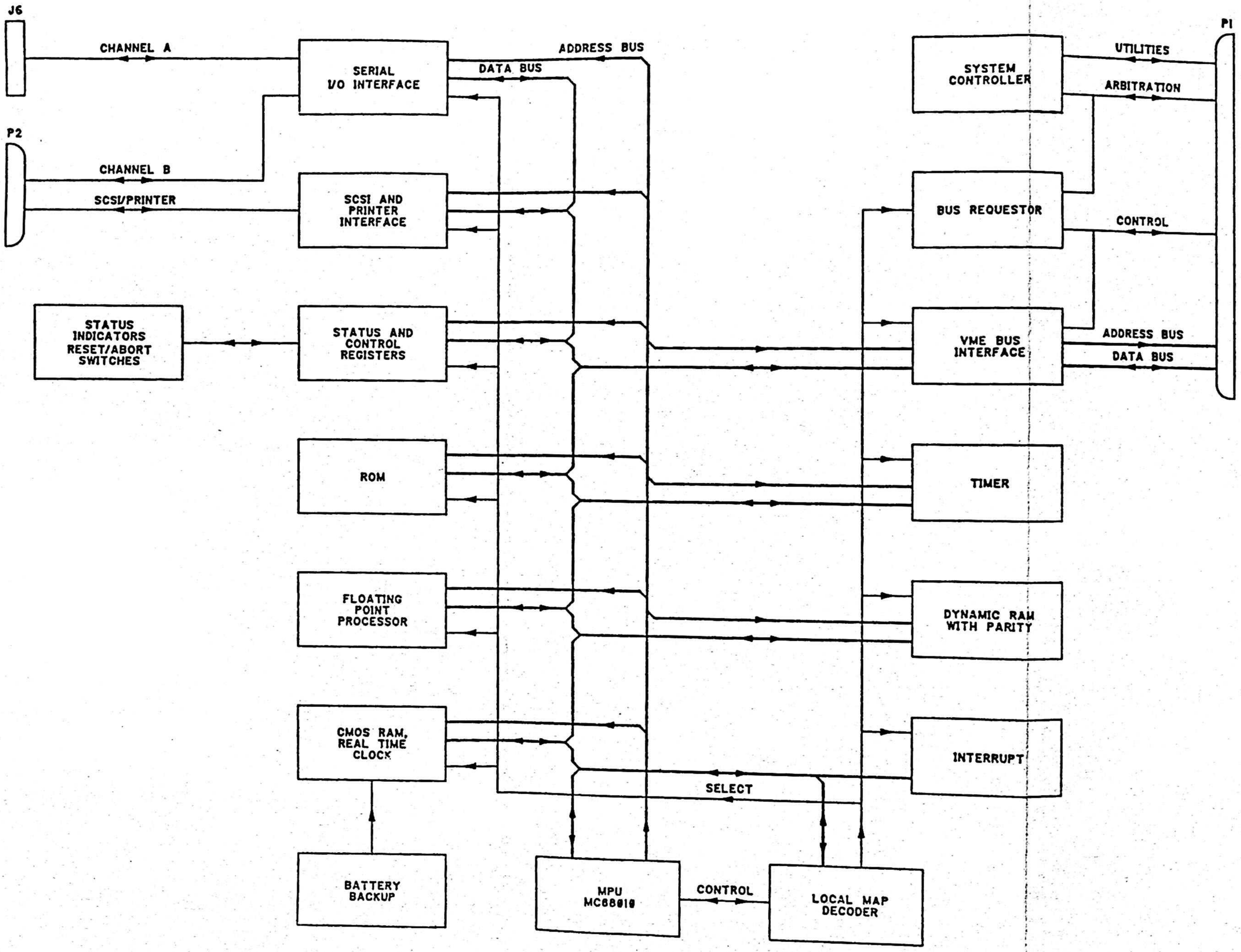

J6
CHANNEL A
SERIAL I/O INTERFACE
ADDRESS BUS
DATA BUS
SYSTEM CONTROLLER
UTILITIES
ARBITRATION
P1
P2
CHANNEL B
SCSI/PRINTER
SCSI AND PRINTER INTERFACE
BUS REQUESTOR
CONTROL
STATUS INDICATORS RESET/ABORT SWITCHES
STATUS AND CONTROL REGISTERS
VME BUS INTERFACE
ADDRESS BUS
DATA BUS
ROM
TIMER
FLOATING POINT PROCESSOR
DYNAMIC RAM WITH PARITY
CMOS RAM, REAL TIME CLOCK
INTERRUPT
SELECT
BATTERY BACKUP
MPU MC68010
CONTROL
LOCAL MAP DECODER

Figure 3-3. CPU Board Block Diagram.

3.4.2 RAM

The CPU board contains 512 Kbytes of RAM, in the form of 18 256K x 1 chips. The RAM array consists of one bank for odd bytes and one bank for even bytes. Dynamic RAMs (150ns access time) are used with 256-row, four milliseconds refresh. Parity on a byte boundary is updated on every write cycle to the on-board RAM. On a read cycle, parity is checked for odd parity. When parity is enabled, the onboard RAM access time is automatically increased to accomodate the additional time required for the parity check. This results in one wait cycle operation from on-board RAM when parity is enabled, and zero wait cycle operation when parity is disabled. Parity checking is performed on both the lower and upper bytes of a word in the RAM whether either or both bytes are read.

3.4.2.1 Refresh. The dynamic RAM is refreshed once every 30 us with two RAS-only refresh cycles. During the refresh operation, all on-board processing stops.

3.4.2.2 Local Access. The local dynamic RAM starting address is 0. The upper address lines are decoded to decide if the cycle is for on-board RAM. If the RAM is selected, the RAM refresh sequencer is started.

3.4.3 BUS REQUESTER

The Bus Requester requests the VMEbus Mastership (see paragraph 2.4, or refer to the VMEbus specification) on one of four bus request levels, and supports the daisy-chain on bus grant. The bus requester operates in the Release-On-Request (ROR) mode or in the Release-When-Done (RWD) mode, and requests bus mastership only if the CPU attempts a VMEbus access and does not already have the bus mastership. The bus mastership is released when a bus request is received on any level or if an on-board refresh sequence is started (ROR), or is released when the CPU is done with the current cycle (RWD). The mode of the bus requester is selectable through bit D0 of the module control register at address $F44007.

3.4.4 INTERRUPT HANDLER

The interrupt handler receives interrupt requests from the serial ports, watchdog timer, SCSI interface, parallel port, ABORT switch, real-time clock, and the seven VMEbus interrupt request lines. All on-board interrupts are disabled at reset until software sets the interrupt-enable bit in the control register. On an interrupt acknowledge cycle, the interrupt handler will supply a vector number from a PROM for an onboard interrupt source (except the serial port interface chip, which supplies its own interrupt vector number), or receive the vector number from the VMEbus for a VMEbus acknowledge cycle. Table 3-1 lists the various interrupt sources and interrupt levels.

Table 3-1. CPU Board Interrupt Sources

INTERRUPT SOURCE	INTERRUPT LEVEL	VECTOR SOURCE	VECTOR NUMBER	OFFSET FROM VBR
ABORT switch	7	PROM	$1F (NOTE)	$7C
AC-Fail	7	PROM	$40 (NOTE)	$100
Serial Ports	6	SIO Chip	programmable	
Timer	5	PROM	$41 (NOTE)	$104
Parallel Port	4	PROM	$42 (NOTE)	$108
Time-of-day clock	3	PROM	$43 (NOTE)	$10C
SCSI Interface	2	PROM	$44 (NOTE)	$110
SYSFAIL	1	PROM	$45 (NOTE)	$114
Reserved for SCSI firmware	--	--	$46	$118
VMEbus IRQ 7	7	VMEbus	supplied	
VMEbus IRQ 6	6	VMEbus	supplied	
VMEbus IRQ 5	5	VMEbus	supplied	
VMEbus IRQ 4	4	VMEbus	supplied	
VMEbus IRQ 3	3	VMEbus	supplied	
VMEbus IRQ 2	2	VMEbus	supplied	
VMEbus IRQ 1	1	VMEbus	supplied	

3.4.5 SERIAL PORTS

Two serial ports are provided by the Z8530A Serial I/O (SIO) chip. One port (Port 2 : Channel B) provides a multi-protocol serial I/O for use with the keyboard interface. The second port (Port 1 : Channel A) is asynchronous, and is accessible on the CPU board front panel at connector J6. Both ports use RS-232C protocol, and the baud rates are programmable in software. In the SCRIBE system, Port A is used for the diagnostic terminal (optional), and Port B is used for the keyboard interface.

3.4.6 TIMERS

Three independant 16-bit timers are provided on the CPU board. Two of these timers are chained through hardware to provide the tick/watchdog timer functions. Timer #3 uses a 1 MHz or 125 KHz internal reference and is used as the "tick" timer for task switching operations. Timer #1 (watchdog timer) shares a register with Timer #3.

3.4.7 SCSI CONTROLLER

The SCSI (Small Computer, System Interface) is based on the NCR 5380 SCSI controller chip. This interface is implemented as specified by the ANSI X3T9.2. The single-ended, open-collector version of the SCSI bus is used. The controller supports bus arbitration including reselection, and operates in both the initiator and the target modes, as defined in the SCSI specification.

All command/status interlacing and data transfers are performed through the NCR 5380. When data is to be transferred, or the SCSI bus is to be acquired, the information is sent to the interface chip which posts an interrupt when processor intervention is required. When the module has been selected by another SCSI bus device, or data is received, an interrupt occurrs allowing the CPU to transfer data to RAM or to act on being selected. The data path is single-buffered on the SCSI controller chip.

The SCSI interrupt to the processor can be disabled through bit D1 of the module control register at address $F44007.

3.4.8 ROM LOCATIONS

Two 28-pin chips (32K x 8 bits each) contain the major on-board firmware for the SCRIBE system. The memory locations for these ROMs are mapped continuously from location $F00000. After a manual CPU board reset, the ROMs are on the first four CPU cyles, in which the CPU fetches its stack pointer and program counter.

3.4.9 TIME-OF-DAY CLOCK

The CPU board uses a MM58274 Real-Time clock chip to provide timekeeping functions for the SCRIBE system. It is programmed to post interrupts to the CPU at specified intervals, and has a 4-bit data bus (using CPU data lines D00-D03). Battery back-up is provided to maintain timer operation when the main power is shut down.

3.4.10 NON-VOLATILE RAM

The CPU board contains CMOS RAM chip U81, which is an 8K X 8 bit memory device. The non-volatile RAM is interfaced to odd-byte data lines D0-D7. This is non-executable memory.

3.4.11 BATTERY BACKUP SYSTEM

The CPU board contains a lithium-battery backup system. This system keeps the Real-Time clock and non-volatile RAM active while main power is shut down. Circuitry is provided to isolate the clock and the RAM from false writes during power-up and power-down. Shelf life of the lithium cell is estimated at five years, and typical operating life of the battery is estimated at three years. A complete procedure for replacing the lithium battery is contained in Section 6 of this manual.

3.4.12 PARALLEL/PRINTER PORT

This subsystem is currently used in the SCRIBE system for V DRIVE interrupts. If the user wishes to connect a Centronics compatible printer, he must purchase the optional serial/parallel board. For more information consult CHYRON Telesystems Sales Department.

3.4.13 FLOATING-POINT CO-PROCESSOR

The CPU board supports a floating point processor (optional). This option provides an IEEE-compatible floating point format and math functions such as add, subtract, multiply, divide, sine, cosine, tangent, square root, powers, and others. For more information about configuring the SCRIBE with the floating-point processor chip, contact the CHYRON Customer Service Department.

3.4.14 SYSTEM CONTROLLER FUNCTIONS

The system controller functions include a 16 MHz system clock, a single-level VMEbus arbiter, system reset (switch and power-up), and a VMEbus time-out generator.

3.4.14.1 Bus Arbiter. The single level arbiter receives level 3 (only) bus requests from the VMEbus and issues a Level 3 (only) bus grant when the bus busy signal is deactivated.

3.4.14.2 Reset Generator, Power Up Reset. The power-up reset generates a local and a system reset for approximately 300 milliseconds. The RESET switch has the same function as the power-up reset except it is initiated by the front panel button. A disable jumper is provided on J7 to disable the front-panel reset switch. Reset can also be generated by the Remote Reset terminals of the External Connections socket. A bit in the Module Status register is set during a power-up reset. This software flag can be used to distinguish between a power-up reset and a user reset for cold restart or warm restart. The module status register at address $F44009 is reset when the ERRCLR location at $F4400F is selected. System reset is enabled by the system controller jumper on J1.

3.4.14.3 System Clock. The 16 MHz SYSCLK signal is provided to the VMEbus by the CPU board. The timing reference is an on-board crystal oscillator, Y2.

3.4.14.4 VMEbus Time-Out. The VMEbus time-out function activates a bus error if a VMEbus cycle exceeds approximately 120 microseconds.

3.5 DISK STORAGE SYSTEMS

3.5.1 DISK CONTROLLER

The SCRIBE system disk controller is a microprocessor-based controller with on-board data separation logic. The controller can handle 5.25" Winchester hard disk drives, multiple floppy-disk drives, and 1/4" tape drives.

The disk controller consists of a single-sided printed-circuit board, which measures 5.75" X 8.0".

Commands to the controller are issued over a bi-directional SCSI bus which allows communication between the disk controller and the SCSI controller (located on the CPU board). The data separator performs serialization/deserialization of data. The operation converts data from the SCSI bus to serial MFM data for writing to disk media, and converts MFM data read from the media into 8-bit bytes for the SCSI bus.

Due to the approach used in the disk controller, the board has extensive diagnostic capabilities. The methodology used increases fault isolation efficiency, thereby reducing system downtime. Error detection/correction is based on a 32-bit ECC polynomial method.

The basic controller can handle a maximum of four disk drives. The board will support up to two Winchester-type hard disk drives, plus two 5.25" floppy disk drives. In addition, the disk controller can be configured to handle various combinations of hard, floppy, and tape storage systems.

3.5.1.1 Controller Features. The following features of the Disk Controller are used in the SCRIBE system.

- Automatic Seek and Verify
- Consecutive Sector Transfers
- Multiple Block Transfers
- Automatic Head and Cylander Switching
- On-board Sector Buffer
- Alternate Track Assignment
- Data Error Sensing and Correction
- Fault Detection

3.5.1.2 **Controller Interface Connections.** Figure 3-4 is a block diagram of a typical system configuration. The SCRIBE VMEbus connects to the disk controller through the Transition Board. The Transition board ensures signal compatibility between the disk controller and the CPU board.

The Winchester Disk Drive Control Interface exchanges status and control information between the controller and the hard disk drive(s). This interface is daisy-chained to each drive attached to the controller, with a terminator installed in the last physical disk drive connected to the chain.

Disk drive parameters, such as the maximum number of cylinders and heads, are passed to the controller over the SCSI bus. This allows disk drives with different characteristics to be attached concurrently to the controller.

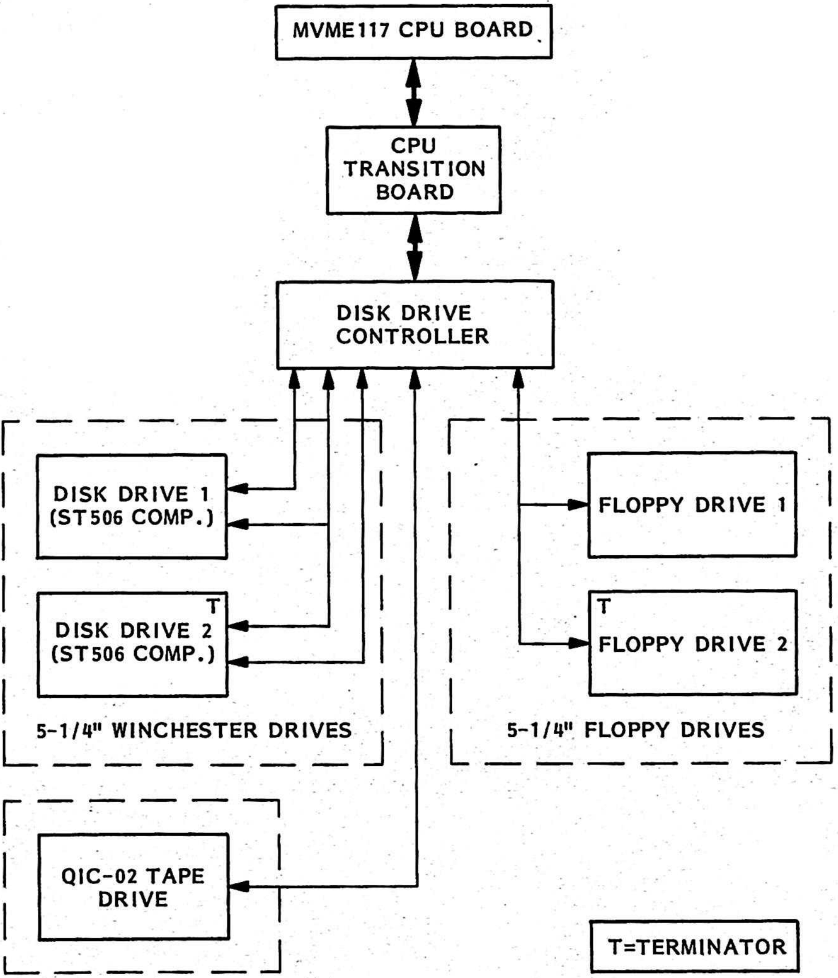

MVME117 CPU BOARD
CPU TRANSITION BOARD
DISK DRIVE CONTROLLER
DISK DRIVE 1 (ST506 COMP.)
T
DISK DRIVE 2 (ST506 COMP.)
5-1/4" WINCHESTER DRIVES
FLOPPY DRIVE 1
T
FLOPPY DRIVE 2
5-1/4" FLOPPY DRIVES
QIC-02 TAPE DRIVE
T=TERMINATOR

Figure 3-4. Disk Subsystem Configuration Block Diagram

The Winchester Disk Drive Data Interface has a separate cable for each disk drive. This interface exchanges serial MFM data between the controller and the selected disk drive.

The Flexible Disk Drive Interface exchanges data and control information between the controller and the disk drive(s). This interface is daisy-chained to each attached disk drive, with a terminator installed in the last physical drive on the chain.

3.5.1.3 **System Configuration.** The SCRIBE VMEbus is connected to the Disk Controller through a SCSI/SASI interface, which is present on the CPU Transition Board. The disk controller connects to the transition board through a 50-line cable which originates at location J1 of the controller board. The pinout for the J1 connector is shown in Table 3-2.

Table 3-2. CPU Transition Board
J1 Connector Pinout

SIGNAL	J1 PIN #	SIGNAL	J1 PIN #
DATA0	2	GND	28
DATA1	4	GND	30
DATA2	6	ATN (not used)	32
DATA3	8	GND	34
DATA4	10	BUSY	36
DATA5	12	ACK	38
DATA6	14	RST	40
DATA7	16	MSG	42
PARITY	18	SEL	44
GND	20	C/D	46
GND	22	REQ	48
GND	24	I/O	50
GND	24		

NOTE: All signals are negative true, and all odd pins on J1 except Pin 25 are connected to ground. The signals lines are terminated with 220-ohms to +5 volts, and 330 ohms to ground.

The hard disk drives are connected to the controller through locations J2, J3, and J4 on the controller board. J2 is a 34-pin header connector which connects all hard disk drives in a daisy-chain configuration. This cable carries control information for the fixed disk drives.

The floppy disk drives are connected to the controller through location J7, which is a 34-pin header connector.

3.5.2 HARD DISK DRIVES

The hard disk drive(s) used in the SCRIBE system are Seagate ST225 drives. The Seagate ST225 Winchester-type hard disk drive provides the SCRIBE user with over 20 megabytes of formatted storage, in a half-height, shock-resistant package. High reliability is assured through the use of a single printed-circuit board, mini-monolithic heads, and oxide media. The drive uses a proprietary helical-band rotary-actuator, which provides excellent thermal stability over the drive's operating temperature range of 50° to 113°F (10° to 45°C). A dedicated head shipping zone assures data integrity during shipping and handling. The ST225 has a MTBF (mean time between failures) of over 20,000 power-on hours. For technical specifications on the Seagate ST225 hard disk drive, consult the manufacturer's literature.

3.5.3 FLOPPY DISK DRIVES

The floppy disk drives used in the SCRIBE is a Panasonic JU-475-2 dual-density, double-sided drive which uses 5.25-inch diskettes. The maximum data transfer rate of the floppy disk drive is 500kbits/second, and formatted SCRIBE diskettes can store up to 1.2 megabytes of data. The drive uses single-element glass-bonded ceramic read/write heads with tunnel erase elements to provide space between recorded tracks. If high-quality medi is used for the disk, no head cleaning or replacement is necessary for the lifetime of the drive. For technical specifications on the Panasonic JU-475-2 floppy disk drive, consult the manufacturer's literature.

Segate
ST-225 $425 (20 meg.)
ST-251 $600 (42/43 meg.)

800-468-3472 (Tech Supp.)
Seagate Technologies

3.6 DUAL-PORTED MEMORY BOARD (FONT MEMORY BOARD)

3.6.1 INTRODUCTION

The dual-ported memory board is the font memory of the SCRIBE. The board uses 256K DRAM SIMM (single, in-line memory module) technology, and is expandable up to 2M bytes in 512k byte increments. The board can be written to or read from over either the VMEbus or the VMXbus. Odd parity is generated for each byte which is written to RAM, and is checked during each read cycle. A 74F764 dual-ported RAM controller performs arbitration, memory address multiplexing, and control signal generation. The board can generate a VMEbus interrupt upon detection of a parity error, and provides information to the CPU board concerning the status of the memory access cycle that was in progress at the time of the error. The dual-ported memory board can be divided into six logical elements. These are:

- VMEbus Interface
- VMXbus Interface
- Arbitration Logic
- Memory Array
- Data Path
- Control Status Register/Interrupter

A functional block diagram of the Dual-Ported Memory Board appears in Figure 3-5.

3.6.2 VMEbus INTERFACE

The VMEbus interface can be described in terms of its three major functions. These are:

- Address Latches and Address Decoding PALs
- Control Signal Drivers/Receivers
- Data Bus Tranceivers

3.6.2.1 Address Decoding. The VMEbus master (CPU board) will allow the address modifier lines and the 24 address lines to set-up on the bus a minimum of 35 ns before AS* is brought low. The address modifier codes propagate through buffer U62 and are presented as inputs to PAL U48. At this point, PAL U48 begins to decode the address modifier lines in order to enable the appropriate output. Signal ENVDCD* is necessary to enable PAL U47 to generate VMEREQ*.

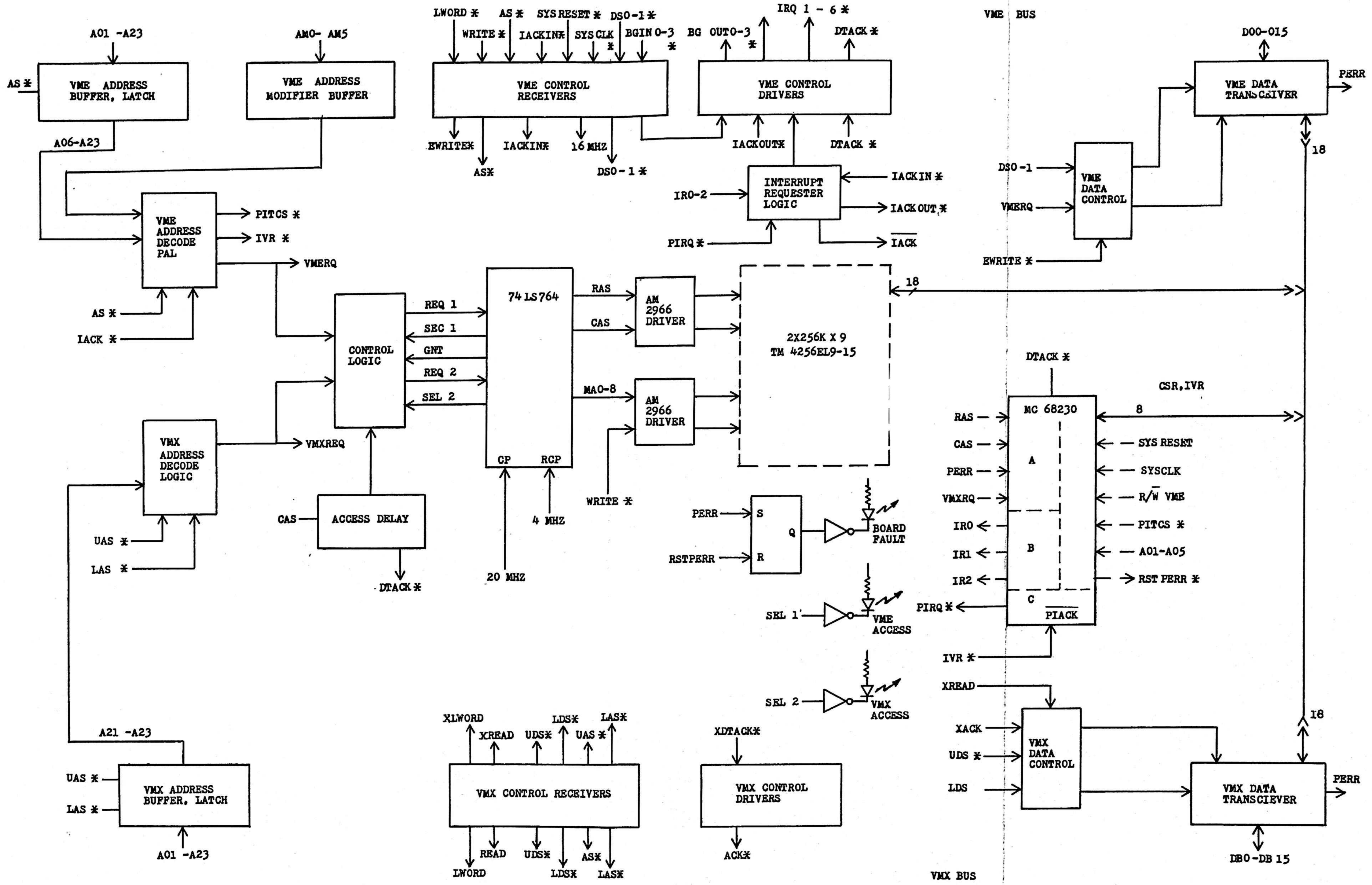

VME BUS
VMX BUS
A01 -A23
AS *
VME ADDRESS BUFFER, LATCH
A06-A23
AM0- AM5
VME ADDRESS MODIFIER BUFFER
LWORD *
WRITE *
AS *
IACKIN*
SYS RESET *
SYS CLK *
DS0-1 *
BGIN 0-3 *
VME CONTROL RECEIVERS
EWRITE*
AS*
IACKIN*
16 MHZ
DS0 - 1 *
BG OUT0-3 *
IRQ 1 - 6 *
DTACK *
VME CONTROL DRIVERS
IACKOUT*
DTACK *
IR0-2
INTERRUPT REQUESTER LOGIC
IACKIN *
IACK OUT *
IACK
PIRQ *
D00-015
VME DATA TRANSCEIVER
PERR
18
DS0 -1
VMERQ
VME DATA CONTROL
EWRITE *
VME ADDRESS DECODE PAL
PITCS *
IVR *
VMERQ
AS *
IACK *
CONTROL LOGIC
REQ 1
SEC 1
GNT
REQ 2
SEL 2
74 LS764
CP
RCP
20 MHZ
4 MHZ
RAS
CAS
MA0-8
AM 2966 DRIVER
AM 2966 DRIVER
WRITE *
2X256K X 9
TM 4256EL9-15
18
VMX ADDRESS DECODE LOGIC
VMXREQ
UAS *
LAS *
CAS
ACCESS DELAY
DTACK *
PERR
RSTPERR
S
R
Q
BOARD FAULT
SEL 1
VME ACCESS
SEL 2
VMX ACCESS
DTACK *
CSR, IVR
MC 68230
8
A
B
C
RAS
CAS
PERR
VMXRQ
IR0
IR1
IR2
PIRQ *
PIACK
SYS RESET
SYSCLK
R/W VME
PITCS *
A01-A05
RST PERR *
IVR *
XREAD
XACK
UDS *
LDS
VMX DATA CONTROL
VMX DATA TRANSCIEVER
PERR
18
DB0 -DB 15
A21 -A23
UAS *
LAS *
VMX ADDRESS BUFFER, LATCH
A01 -A23
XLWORD
XREAD
UDS*
LDS*
UAS *
LAS*
VMX CONTROL RECEIVERS
LWORD
READ
UDS*
LDS*
AS*
LAS*
XDTACK*
VMX CONTROL DRIVERS
ACK*

Figure 3-5. Dual-Ported Memory Functional Block Diagram

If a Standard Supervisory Program or Data Access address modifier code is placed on the bus, output ENVDCD* will go active. This output will also go active if a Standard Non-Privileged Program or Data Access code is placed on the bus, provided that the /DSAUSER line has not been activated. This line is used to disable User mode accesses to the board's resources.

Once the address lines have set-up, the VMEbus master will assert AS*, which latches the 24 address lines into latches U60, U61, and U63. The combination of ENVDCD* active, EAS*, and a combination of $06 or $07 on address lines EA23 - EA20 will activate VMEREQ*.

If a Short address modifier code (2D$ or 29$) is present, ENVDCD* will not be asserted (by U48). Instead, ENPDCD* will be asserted, provided that user mode accesses have not been disabled. If user mode accesses have been disabled, then an address modifier code of 29$ will not be responded to.

A short address modifier code informs a slave device that only sixteen address lines are to be decoded. This decoding is performed by PAL U46. Since the MC68230 Parallel Interface/Timer (PI/T) used as the board's control status register (CSR) has been assigned short address space FF0001 through FF003F, PAL U46 wants to see EA06 through EA15 low. If these lines are low, EAS* is active and ENPDCD* is active, then PITSEL* will be asserted to select the PIT.

Delay line DL3 is used to delay the address strobe for various timing needs. Two of its 30ns taps are used.

3.6.2.2 Control Signal Drivers/Receivers. The VMEbus grant inputs are looped over to the bus grant outputs because they are unused and must be daisy-chained. U64 receives the VMEbus data strobes, write line, interrupt acknowledge input, system reset, and 16 MHz system clock.

Signal IACK* is received by U62 and is presented to PAL U48. This signal is ANDed with the address strobe to form signal INTACKCYC*, which is used by the interrupter circuitry.

U58 is an open-collector driver that is used to drive DTACK* (data transfer acknowledge) onto the VMEbus.

3.6.2.3 Data Transceivers. Two AM29853 Parity Bus Transceivers (U65, U66) are used to drive and to receive the data bus. Odd parity is generated for each byte that is written to RAM. This parity bit is stored along with the data and is checked when the byte is read. If a parity mismatch is detected, pin 10 of (U66, U65) is asserted to signify a parity error. PALs U29 and U21 generate the control signals for these transceivers. Signal ENExTR* is asserted during write cycles and ENExRC* is asserted during read cycles. Signal ENExPE* is asserted when data is valid and is used to enable parity checking.

Byte 0 corresponds to D00 - D07 (odd addresses) and Byte 1 corresponds to D08 - D15 (even addresses). Both transceivers are enabled for data word accesses.

Signal RSTPERR* is asserted under program control when it is desired to reset the AM29853 parity error latches.

3.6.3 VMXbus INTERFACE

The VMXbus interface is used to communicate between the dual-ported memory board and the BMPU graphics processor. This interface can be divided into three logical elements:

- Control/Address Receivers
- Address Latches/Decoders
- Data Bus Transceivers

3.6.3.1 Control and Address Receivers. Buffers U52 and U53 receive the VMXbus multiplexed address bus, as well as data and address strobes. One gate from U55 is used to buffer the VMX READ signal.

The source of UAS* can be either P2, C9 or P2, C27. The positioning of jumper JL3 determines which bus pin is used. The VMXbus specification dictates that UAS* be run on P2, C27; however, the SCRIBE backplane uses P2, C9 to protect this signal from RF and associated interference. Jumper link JL2 (shown in Figure 3-6) is factory installed in the 2-4 position.

JL3

```
2  | []==[] |  4
   |        |
1  | []  [] |  3
```

UAS* source	JL3 Pins
P2, C27 (Standard VMX)	1 - 3
P2, C9 (SCRIBE)	2 - 4

Figure 3-6. UAS* Source Selection

3.6.3.2 **Address Latches/Decoders.** Address information on the VMXbus is provided in two phases. The first phase uses the 12 address lines to provide the lower half of the 24-bit address. The lower address is clocked into registers U39 and U54 on the low to high transition of XLAS* (VMX Lower Address Strobe). The second phase provides the upper address and the assertion of XUAS* (VMX Upper Address Strobe). XUAS* latches the upper 12 bits of the address information.

XUAS* is delayed by DL2. Once XUASDLY2 becomes active, PAL U25 begins to decode the upper four address lines. If the VMX address falls within the board's 2Mbyte boundary, a VMXREQ* will be asserted.

3.6.3.3 **Data Bus Tranceivers.** Parity bus tranceivers are also used on the VMXbus. Refer to the VMEbus interface description, paragraph 3.6.2.3, for a description of data bus tranceiver operation.

3.6.4 ARBITER/DRAM CONTROLLER

When a VMEREQ* is presented to PAL U28, signal SREQ1* will be asserted and will cause flip-flop U26 to set. This action will cause REQ1* to be presented to pin 21 of U15. A similar sequence of events occurs when a VMXREQ* is desired. Requests for VMX accesses are presented to U15 pin 22 as REQ2*.

The 74F764 performs arbitration, control signal timing, address latching and multiplexing, and refresh cycle generation.

Arbitration between the two bus requests takes place on different edges of clock RCP. VMEbus requests are sampled on the rising edge of RCP, and VMX requests are sampled on the falling edge.

When the 74F764 detects a request, it generates the appropriate select output (SELE* for VME, SELX* for VMX). If there is no refresh request pending, the 74F764 asserts the GNT signal. The rising edge of GNT clocks flip-flop U13. P1CYCLE will go high if the current access cycle is a VME cycle. P2CYCLE will be asserted if the current access cycle is a VMX cycle. Only one of these two signals should be active at any given time.

The select inputs on address multiplexers U41 through U45 are controlled by the level of signal SELX. The respective address lines propagate through the multiplexers and are presented to the address inputs of U15. When GNT goes active, RAMAD01 through RAMAD18 are latched internally by U15, and the state of RAMAD19 and RAMAD20 is clocked into U11. The 74F764 allows RAMAD01 through RAMAD09 to propagate to the MA outputs. GNT* also enables U9, which allows DPLDS*, DPUDS*, and DPWR* to be enabled if required. At this point, the respective Data Tranceivers are enabled.

On the next edge of RCP, RASEN* is triggered. This signal propagates through 74F08 U22 and becomes PRAS*, which is input to AM2966 chip U19. At this time, RAS0* through RAS3* are enabled. The DRAMs then strobe in the row address.

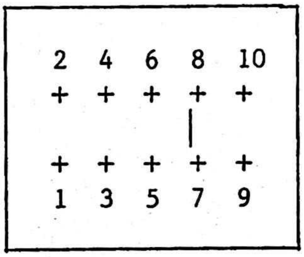
After the next edge of RCP, WGATE is triggered. This signal enables 74F10 chip U18, which provides WEL* and WEH* to the DRAMs for an Early Write Cycle, if the current cycle is a write cycle. Also at this time RAMAD10 through RAMAD18 are allowed to propagate through to the MA bus. On the next edge of RCP, CASEN* is triggered, which toggles flip-flop U10, enabling CAS*. CAS* is OR'ed with RASEN* to enable PRAS* throughout the entire cycle.

When CAS* goes active, 74F139 chip U16 enables the output selected by the state of RAMAD19 and RAMAD20. The outputs of U16, C0* through C3*, are the inputs to driver U17. C0* through C3* are also run to the MC68230 port A inputs. These are used for parity error status capture.

Three RCP cycles later, RASEN* is negated. After this state, all outputs of U15 are maintained until the request is removed.

After CASEN* is enabled, it is inverted and run through a 30ns-per-tap delay line. The RAM access time is determined by the time between assertion of CAS* and output data valid, TAC. The -15 (150ns) DRAMs have a maximum TAC of 75ns. The 90ns tap provides the correct access time for -15 and -12 DRAM modules. To use -20 DRAMs, the 120ns tap must be used. Header JL2 (shown in Figure 3-7) is used to select this delay value. (The board is factory shipped with JL2 jumper in the 7 - 8 position.)

JL2



Access Time Value	JL2 Pins
120ns from CAS	1 - 2
60ns	3 - 4
180ns	5 - 6
90ns	7 - 8
30ns	9 - 10

Figure 3-7. DRAM Access Time Select

Shift register U33 ensures that the data has been valid for a minimum time, TDH, before an acknowledge is enabled during write cycles.

EACK is used as the transfer acknowledge for VMEbus accesses and XACK for VMXbus accesses. PAL U21 is used to enable parity checking during read cycles. Parity checking is performed after the associated acknowledge becomes active.

3.6.5 MEMORY ARRAY

The memory array of the dual-ported memory board consists of up to eight 256k x 9 bit DRAM modules. The multiplexed address bus is driven by AM2966 chips U30 and U17.

U17 is also responsible for driving the column address strobes and write enable lines. U19 is responsible for driving the row address strobes. The following table (Table 3-3) can be used to map out the appropriate memory module if an error occurs:

Table 3-3. Memory Array Module Map

VME Address	VMX Address	Row Address Strobe	Column Address Strobe	Byte	DRAM Module	Total Resident RAM
600000- 67FFFF	0- 7FFFF	RAS0*	CAS0*	Low (odd) High (even)	U1 U2	512k
680000- 6FFFFF	80000- 8FFFF	RAS1*	CAS1*	Low High	U3 U4	1M
700000- 77FFFF	90000- 97FFF	RAS2*	CAS2*	Low High	U5 U6	1.5M
780000- 7FFFFF	98000- 9FFFF	RAS3*	CAS3*	Low High	U7 U8	2M

3.6.6 DATA PATH

The data path between either bus and the memory array consists of AM29853 Parity Bus Transceivers. These chips generate odd parity, which is delivered to RAM on signals PD00 and PD01. Only one bus will be enabled at a given time.

During memory write operations, the transmit enable input (pin 14) is activated by PAL U29. During read cycles, the receive enable input (pin 1) is enabled. The parity bit is checked during read cycles by asserting the enable latch input (pin 13). The parity error latch is cleared by asserting the clear input (pin 11).

Table 3-4 shows the function of PAL chip U29.

Table 3-4. PAL U29 Data Path Decoding Fucntions

VME	VMX	Read	Write	LDS	UDS	Active Output
1	0	0	1	0	1	ENE1TR
0	0	1	0	0	1	ENE1RC
1	0	0	1	1	0	ENE0TR
1	0	1	0	1	0	ENE0RC
0	1	0	1	0	1	ENX1TR
0	1	1	0	0	1	ENX1RC
0	1	0	1	1	0	ENX0TR
0	1	1	0	1	0	ENX0RC

Note: 1 = Active or True
0 = Inactive or False

A parity error can be forced for diagnostic purposes. The AM29853 transceivers guarantee that incorrect parity will be generated when both the transmit and receive enables are active. PAL U29 will do this if input FRCPERR* is asserted. This signal is under software control as an output from the PI/T.

PAL U21 is responsible for generating the parity checking enables. Parity is checked during read cycles when output data from the DRAMs is valid.

3.6.7 CSR/INTERRUPTER

The control status register and interrupter module is based on the MC68230 Parallel Interface Timer (PI/T). This device resides on the VMEbus Short Address Space. Requests to the PI/T device and the address decoding that occurs is explained in the VMEbus interface description in paragraph 3.6.2.

The PI/T is connected to VMEbus data lines D00 - D07 via 74LS645-1 tranceiver U67. The VMEbus WRITE* signal provides the direction control for the transceiver. U67 is tri-state enabled during both read/write accesses abd during interrupt acknowledge cycles where the PI/T is the interrupter being acknowledged.

The following events occur when a parity error is detected by the AM29853 parity bus transceivers:

1) A parity mismatch is detected by whichever transceiver is enabled. The respective error line, PERR0* or PERR1*, is asserted. PERR0* is asserted if the error was on MD0 - MD7, and PERR1* is asserted if the error was on MD8 - MD15.

2) PAL U36 sees either error line asserted. U36 then asserts signal ERROR, which is inverted and applied to the H1* input of the PI/T. This causes the column and cycle information to be latched into the port A input buffer register.

   Signal ERROR also enables shift register U50 to begin clocking. After two PCLK cycles, PI/T input H2 is driven high. The PI/T is programmed to generate an interrupt request upon detection of H2 true.

3) Signal ERROR is also looped back into PAL U36 via U22, where it is OR'ed with RESET*. PAL U36 is configured internally as an RS flip-flop. This is set when U36 pin 9 is brought low, and is reset when pin 19 is brought low. When U36 is set, pin 16 will be high, and pin 13 will be low. This combination on the input of LED driver U24 will cause the bi-color LED to be red.

4) The desired interrupt level will have been written to PI/T port B during initialization. Pins 19, 18, and 17 of U37 will have a binary representation of the desired interrupt level latched into port B's output buffer. When the PI/T device detects that H2 has gone high, an interrupt request is initiated. The PI/T drives pin 35 low. It is PAL U31's task to assert the correct interrupt request. Table 3-5 illustrates the operation of PAL U31.

Table 3-5. PAL U31 Operation Truth Table

U31 Pin Number:	2	3	4	8	Interrupt Line Generated
Label:	PB2	PB1	PB0	PIRQ*	
	X	X	X	1	NONE
	0	0	0	0	NONE
	0	0	0	0	IRQ1*
	0	1	0	0	IRQ2*
	0	1	1	0	IRQ3*
	1	0	0	0	IRQ4*
	1	0	1	0	IRQ5*
	1	1	0	0	IRQ6*
	1	1	1	0	NONE

5) When the VME Interrupt Handler receives the interrupt, it initiates an Interrupt Acknowledge Cycle. The lower three VMEbus address lines will reflect the level of the IRQ* line that was asserted. The handler then initiates the Interrupt Acknowledge Daisy Chain. The Interrupt Handler (on the CPU board) asserts signal IACK*.

The memory board receives signal IACK* at U62. PAL U48 asserts signal IACKCYC*, which is presented to PAL U31. Signal IACK* propagates through each Interrupter Module in the system via the IACKIN*/ IACKOUT* lines.

6) A VME Interrupter must bypass the interrupt acknowledge daisy-chain signal if it is not requesting that level of interrupt. PAL U31 monitors the three lower address lines and will allow the IACKIN* signal to either propagate through the board if a parity error has not occurred, or allow the PI/T to respond. Flip-flop U23 is cleared whenever EAS inactive. If the parity error interrupt is the interrupt that is being acknowledged, PAL U31 will bring output pin 19 low. If the parity interrupt is not being serviced, pin 19 will be high. EASDLY2, which is responsible for clocking flip-flop U23, is actually EAS delayed by 60ns. Signal ALWIACK is asserted to enable the IACKIN* signal to propagate through to IACKOUT*. Signal ALWPIACK is asserted to enable the PI/T interrupt to be acknowledged.

7) The interrupter must place a status/ID byte on the lower eight data bus lines and signal the byte's validity by asserting DTACK*. Signal PIACK* enables transceiver U67. PIACK* is also presented to pin 36 of the MC68230 (U37). U37, upon seeing PIACK* asserted, places the interrupt vector that has been written to its Interrupt Vector Register on D00 - D07. U37 then asserts PDTACK* (pin 42) to signal the interrupt handler that the status/ID byte is valid. PDTACK* is OR'ed with EACK* to form DTACK*.

3.7 BI-POLAR MICROPROCESSOR UNIT (BMPU) BOARD

The BMPU is a microprocessor-controlled board that reads data stored in the font memory, processes the data into pixel information, and writes this pixel information to the frame buffers for dispaly. The BMPU can be divided into four basic circuit groups (refer to Figure 3-8).

- Microprocessor circuitry
- CPU Interface circuitry (VMEbus)
- Font Memory Interface (VMXbus A)
- Frame Buffer Interface (VMXbus B)

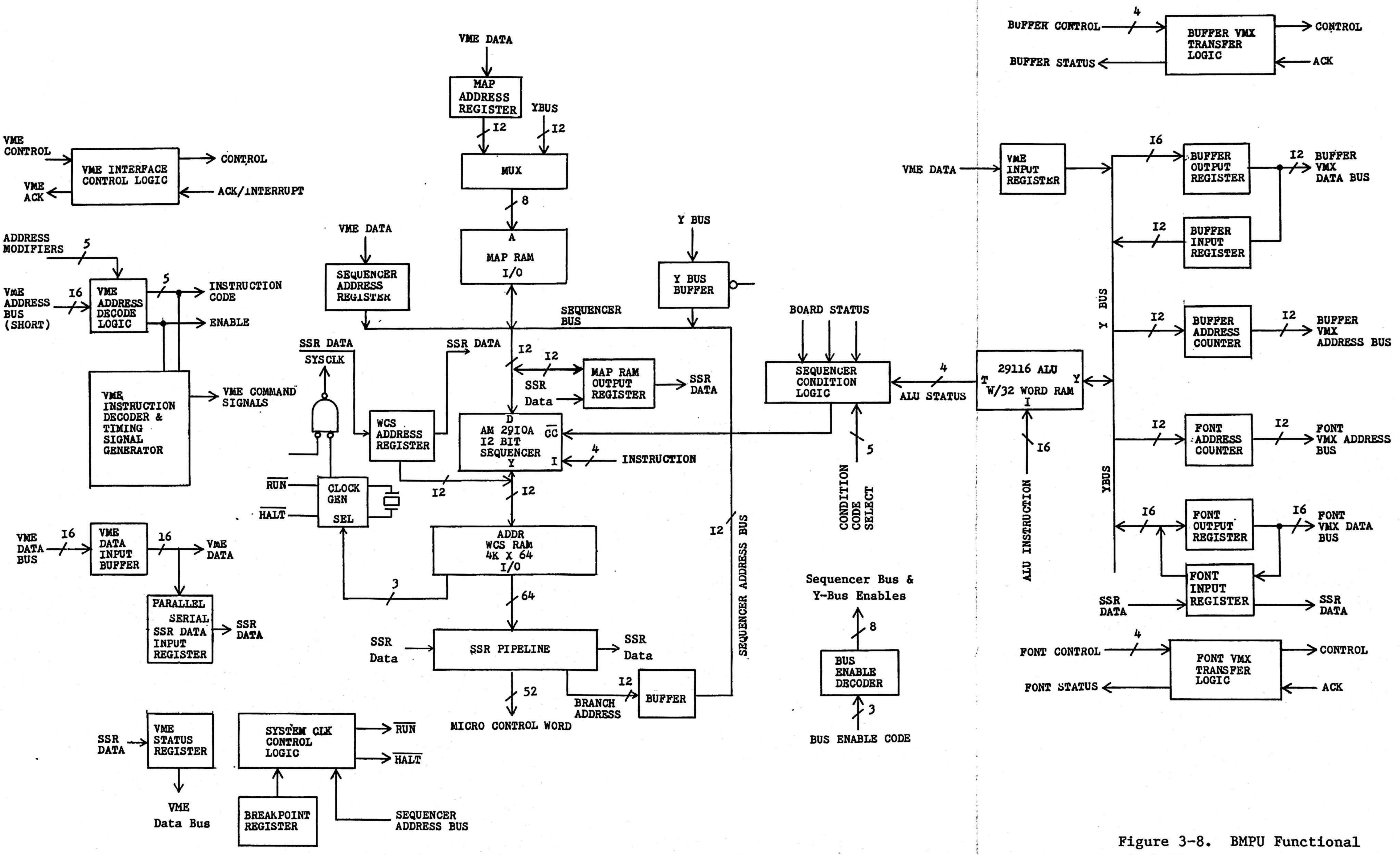

VME CONTROL
VME INTERFACE CONTROL LOGIC
CONTROL
VME ACK
ACK/INTERRUPT
ADDRESS MODIFIERS
5
VME ADDRESS BUS (SHORT)
16
VME ADDRESS DECODE LOGIC
5
INSTRUCTION CODE
ENABLE
VME INSTRUCTION DECODER & TIMING SIGNAL GENERATOR
VME COMMAND SIGNALS
VME DATA BUS
16
VME DATA INPUT BUFFER
16
VME DATA
PARALLEL SERIAL SSR DATA INPUT REGISTER
SSR DATA
SSR DATA
VME STATUS REGISTER
VME Data Bus
SYSTEM CLK CONTROL LOGIC
RUN
HALT
BREAKPOINT REGISTER
SEQUENCER ADDRESS BUS
VME DATA
MAP ADDRESS REGISTER
YBUS
12
12
MUX
8
A
MAP RAM
I/O
VME DATA
SEQUENCER ADDRESS REGISTER
SSR DATA
SYSCLK
SSR DATA
WCS ADDRESS REGISTER
RUN
HALT
CLOCK GEN
SEL
12
12
SSR Data
MAP RAM OUTPUT REGISTER
SSR DATA
D
AM 2910A 12 BIT SEQUENCER
CC
Y
I
4
INSTRUCTION
12
12
3
ADDR WCS RAM 4K X 64 I/O
64
SSR Data
SSR PIPELINE
SSR Data
52
MICRO CONTROL WORD
BRANCH ADDRESS
12
BUFFER
Y BUS
Y BUS BUFFER
SEQUENCER BUS
12
SEQUENCER ADDRESS BUS
BOARD STATUS
SEQUENCER CONDITION LOGIC
5
CONDITION CODE SELECT
Sequencer Bus & Y-Bus Enables
8
BUS ENABLE DECODER
3
BUS ENABLE CODE
4
ALU STATUS
29116 ALU W/32 WORD RAM
T
Y
I
16
ALU INSTRUCTION
VME DATA
VME INPUT REGISTER
Y BUS
YBUS
BUFFER CONTROL
4
BUFFER VMX TRANSFER LOGIC
CONTROL
BUFFER STATUS
ACK
16
BUFFER OUTPUT REGISTER
12
BUFFER VMX DATA BUS
12
BUFFER INPUT REGISTER
12
BUFFER ADDRESS COUNTER
12
BUFFER VMX ADDRESS BUS
12
FONT ADDRESS COUNTER
12
FONT VMX ADDRESS BUS
16
FONT OUTPUT REGISTER
16
FONT VMX DATA BUS
SSR DATA
FONT INPUT REGISTER
SSR DATA
FONT CONTROL
4
FONT VMX TRANSFER LOGIC
CONTROL
FONT STATUS
ACK

Figure 3-8. BMPU Functional Block Diagram

The data stored in the font memory is divided into two basic sections: the display list section and the encoded font data. The display list data is the information that describes characters and their positions on the screen, the color, the font number, and the frame into which it is to be built. On the SCRIBE video screen output there are 24 rows, each containing up to 64 characters.

The encoded font data is the actual run-length data that is decoded by the BMPU to create pixel data. The data is sequential so that the next run-length word corresponds to the next group of pixels seen on the display. All font memory accesses are handled over the font memory (VMXbus A) interface.

The attributes of each character are read from the display list and stored on the BMPU board. The character line and pixel position are then loaded into the frame buffer through the frame buffer interface (VMXbus B). The encoded data is read from the font memory and decoded in the ALU. This is where run-length words are converted into actual pixel data and then written to the frame buffer. All frame buffer accesses are handled by the frame buffer interface and each character is completed before the next character is started.

Additional operations performed by the BMPU are erasing the frame buffer, crawling the buffer, rolling the buffer, and general diagnostics. These functions are basic variations on the standard font memory read/frame buffer write operations.

3.8.1 MICROPROCESSOR CIRCUITRY

All functions of the BMPU are based on its microprocessor logic. This circuitry reads the microcode program that is stored in RAM on the BMPU and executes the instructions. This microcode controls all the hardware involved with reading the font memory, conversion of the data, and writing pixel data to the frame buffers.

The microprocessor circuitry consists of a 2910 microprogram sequencer, a 29116 16-bit ALU, a 4K x 64 bit RAM for the microcode (writable control storage, or WCS), a 2925 programmable microcycle clock controller, a 64-bit wide WCS output pipeline register, a 256 x 12 bit address MAP RAM, and three PALs for microprogram branch control. The sequencer is used as the address generator for the WCS RAMs. The sequencer operates under the control of the microprogram and executes the instructions necessary for program addressing. The microcode, also referable as the WCS, is stored in the WCS RAMs and is addressed by the sequencer. The outputs of the WCS RAMs are latched into the output pipeline register so that the next instruction may be accessed while the curent instruction is being executed. Each instruction contains the bits necessary to control the ALU, the sequencer, the microcycle clock, the branch logic, the branch address, the font interface logic, the frame buffer logic, the VMEbus bus, and the internal data bus outputs. A new instruction is latched into the pipeline register on the rising edge of every clock cycle. The ALU is used to perform the arithmetic calculations necessary for the data conversion and interface routines. The MAP RAMs are provided so that the location of various routines in the microcode can be easily modified via software and they supply a vector address to the input of the sequencer as required.

3.7.2 CPU INTERFACE

The CPU interface is the logic which interfaces the BMPU with the MVME117 CPU board. This interface is a standard VME interface with the BMPU acting as a slave device to the CPU board. This interface is used so that the MVME117 can initially load the BMPU microcode and start the BMPU processor. Once the BMPU is running under control of the microcode, the MVME117 CPU board will instruct the BMPU to do the various higher level commands that involve building the frame buffers, or diagnostics.

The logic consists of VME address latches and decoders, VME data latches and instruction decoders, and PALs which control the interface based on the decoded instructions. The BMPU acknowledges short VME addresses from $FF0300 to $FF0320 where the specific address is decoded as an instruction for the BMPU to execute. The VME data bus provides the data that is required to execute the instruction, if necessary. For high level BMPU instructions such as erase, build, roll, or crawl, the data bits are decoded by the microcode and the appropriate subroutine is called to execute the function.

3.7.3 DUAL PORTED MEMORY INTERFACE (Font Memory)

The dual-ported memory interface is the logic that controls the BMPU accesses to the font memory. The interface is a modified VMX interface with the BMPU as the bus master. The VMX data interchange takes place through the P2 connector on the SCRIBE backplane. The purpose of the interface is to allow the microprocessor logic to simply load the font memory interface with the desired address and have the interface generate the actual timing and handshake signals required for the VMX data transfer. This allows the microprocessor to perform other tasks while the font interface accesses the memory. Once the access has been completed, the interface will set a bit (polled by the microprocessor) which indicates completion.

The circuit consists of one set of address latch/counters, a 16-bit input data register, a 16-bit output data register, and 2 PALs which control the interface. The font memory logic has the ability to read consecutive font memory locations so that the microprocessor will not be required to load a new addess after each access. This feature is especially beneficial for encoded data reads where the data is sequential in nature.

3.7.4 Frame Buffer Interface

The frame buffer interface is the circuit that controls the BMPU accesses to the frame buffer. Like the font memory interface, the frame buffer interface is a standard VMX interface but takes place over the P3 connector on the backplane. The frame buffer address and data are loaded into the interface by the microprocessor, and then the interface generates the proper timing and handshake signals to complete the access. The data word is the pixel information which consists of character color and anti-alias data. The address consists of 10 bits for the scanline position, 10 bits for the starting pixel information, and 4 bits for mode control. The mode bits are used to determine whether the frame buffers are to write the pixel data, erase the given line, or crawl the given line. In addition, the mode bits indicate which frame buffer is to be operated on (one of: Foreground A, Background A, Foreground B, Background B).

This circuitry is essentially similar in design to the font memory interface logic, and contains the same components.

3.8 FRAME BUFFER BOARDS

Paragraph 3.8 has been deleted due to the proprietary nature of the design. Tables 3-6, 3-7, and 3-8 and Figure 3-9, have also been deleted.

3.9 DISPLAY BOARD FUNCTIONAL DESCRIPTION

Paragraph 3.9 has been deleted due to its proprietary nature. Tables 3-9 and Figure 3-10 have also been deleted.

3.10 ANALOG VIDEO SECTION: SYNC GENERATOR, ENCODER

The SCRIBE video processing section is divided into a sync generator/genlock board and an encoder board. Together, these sections perform the task of converting the SCRIBE digital information plus the customer's input video and control signals into viable anti-aliased characters either stand-alone or over the customer's program video.

Refer to Figure 3-11 for Analog Video Section Block Diagram.

3.10.1 SYNC GENERATOR/GEN-LOCK

The sync generator/genlock board is located in Slot 20 of the SCRIBE mainframe card cage, and operates as a gen-lockable sync generator which provides timing pulses to the digital control circuitry as well as the necessary encoding signals to the video encoder section.

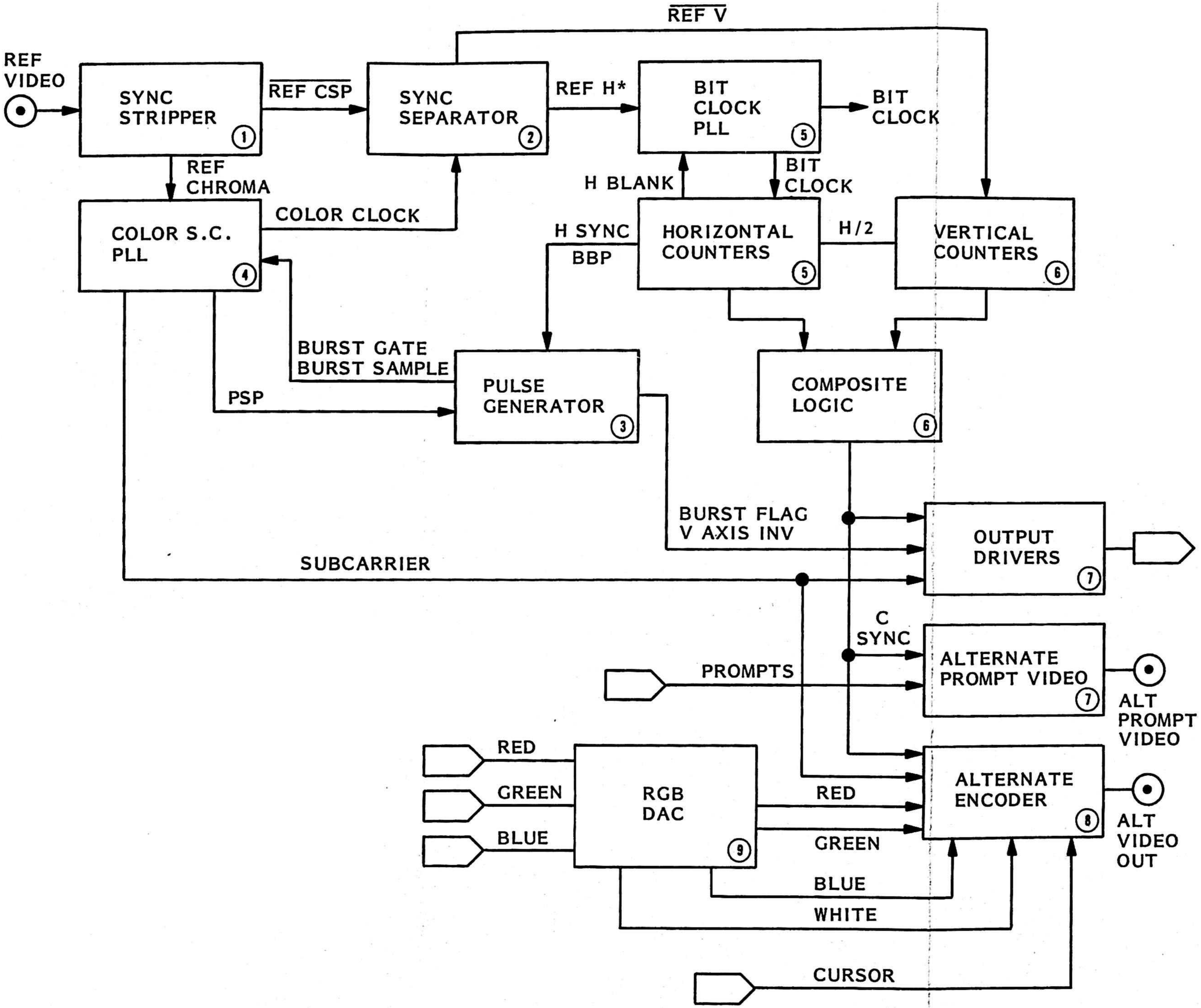

REF V
REF VIDEO
SYNC STRIPPER ①
REF CSP
SYNC SEPARATOR ②
REF H*
BIT CLOCK PLL ⑤
BIT CLOCK
REF CHROMA
H BLANK
BIT CLOCK
COLOR S.C. PLL ④
COLOR CLOCK
H SYNC
BBP
HORIZONTAL COUNTERS ⑤
H/2
VERTICAL COUNTERS ⑥
BURST GATE
BURST SAMPLE
PSP
PULSE GENERATOR ③
COMPOSITE LOGIC ⑥
BURST FLAG
V AXIS INV
OUTPUT DRIVERS ⑦
SUBCARRIER
C SYNC
PROMPTS
ALTERNATE PROMPT VIDEO ⑦
ALT PROMPT VIDEO
RED
GREEN
BLUE
RGB DAC ⑨
RED
GREEN
BLUE
WHITE
ALTERNATE ENCODER ⑧
ALT VIDEO OUT
CURSOR

Figure 3-11. Analog Video Section Functional Block Diagram

Composite video from the customer is input to the SYNC STRIPPER block, which amplifies the signal (Q24, Q30), separates the color subcarrier (Q17, Q20), clamps the luminance (Q18, Q11, Q12, Q13), and strips sync at precisely 50% down the sync pulse (U20). This composite sync signal goes to the vertical detect logic and the 2H eliminate blocks. A burstgate signal is also generated and sent to the burst detect logic where the subcarrier from the input video is regenerated.

The 2H ELIMINATOR block (U33) will eliminate the equalizing pulses from the vertical interval and supply a horizontal sync signal to the phase detector of the horizontal phase locked loop.

The VERTICAL DETECT block (U35) detects the vertical interval and generates a vertical reset pulse for the vertical counters.

The BURST GATE section (Q9, Q10) allows only the reference burst through to the subcarrier phase detector.

The SUBCARRIER PHASE DETECTOR (U23) compares the phase of the burst detector subcarrier with that of the VCO and generates an error voltage to the VCO (Q7, Q8). This error voltage will adjust the phase of the VCO subcarrier until it matches that of the burst detect subcarrier.

The PHASE ADJUST block between the VCO and the phase detector allows the phase of the subcarrier to be adjusted by the operator by 360 degrees.

The PAL PHASE logic is only used for PAL encoding. This logic determines the phase of the V-axis subcarrier and changes it every scanline. A signal from the PAL burst phase detector (U13) will set the 7.8 KHz flip-flop and the H-sync signal from the decoder section will toggle it. Also, this section generates the Bruch burst blanking sequence, per PAL specifications.

The H-PHASE DETECTOR compares the phase of the input sync with the phase of the horizontal sync being generated by the genlock. This comparison generates an error voltage to the horizontal VCO which attempts to keep a fixed phase relationship between them.

The HORIZONTAL VCO (Q34, or piggy-back board on earlier Sync Gen boards) oscillates at 12.14686 MHz for 525-line systems and 14.71875 MHz for 625 line systems. The goal is to have 772 bit clocks for 525 line systems, and 940 bit clocks for 625 line systems. These clocks go to the horizontal counter and the decoder logic which generates the sync signals.

The HORIZONTAL COUNTER (U50, U51, U52) counts the bit clocks and inputs a 10-bit number to the decoder PROM (U64), indicating the current count to the decoder. The horizontal counter must be reset every 772 clocks for 525 line systems and every 940 bit clocks for 625 line systems.

The VERTICAL COUNTER (U37, U38, U39) sends a 10-bit number to the decoder PROM (U40) indicating the current scan line. The counter is reset by the vertical reset pulse from the vertical detect logic. Then, the counter counts horizontal sync pulses to determine the current scanline.

The DECODER logic (U53, U66, U49) will generate the required sync signals to the main system. These signals are:

1. Vertical Drive
2. Burst Gate
3. Odd-field Drive
4. Composite Blanking
5. Composite Sync
6. Horizontal Sync

All of these signals should conform to the appropriate video system standard (either NTSC, PAL, or PAL-M).

The PHASE ADJUST block (U1) from the decoder to the horizontal phase detector is used to time the horizontal phase of the gen-lock source to the input sync. This block allows the horizontal phase to be adjusted from 1.0 us ahead of input sync to 1.0 us after it.

When gen-locking to a video input, horizontal sync will lock to the input sync and subcarrier used for modulation will be locked to the burst signal of the composite video input. If no input is present, the subcarrier crystal oscillator will free run, and the horizontal VCO will lock to it according to the following relationships:

$F_{sc} = (455/2) * F_h$ in the NTSC system

$F_{sc} = (909/4) * F_h$ in the PAL-M system

$F_{sc} = (1135/4) * F_h$ in the PAL system

Note that the PAL subcarrier will not have a 25 Hz offset, in the non gen-lock case.

3.10.1.1 Inputs From The Customer

A) 1 volt peak-to-peak composite video

3.10.1.2 Outputs To CHYRON SCRIBE

A) Horizontal Sync
B) Composite Blanking
C) Vertical Drive
D) Odd/Even Field Drive
E) Bit Clock
F) Vertical Blanking

3.10.1.3 Outputs to Video Encoder

A) Composite Sync
B) Composite Blanking
C) Subcarrier
D) Burstgate
E) V-axis Phase (for PAL encoding)
F) Bit Clock

3.10.1.4 Adjustments Available To Customer

A) H-sync adjust (+/- 1 us from input video)
B) Subcarrier phase adjust (0 to 360 degrees)
C) Vertical phase adjust (± 1 horizontal line)

3.10.2 VIDEO ENCODER

The video encoder section consists of one P.C. board, located on the inside of the SCRIBE mainframe rear door. This section encoders digital RGB data from the digital logic into composite video. The encoder is able to produce colors accurate to within three degrees (3°) of phase and five degrees (5°) of amplitude when viewed on a vectorscope. The encoder is factory configurable for either NTSC or PAL formats.

A 4 bit digital key signal must also be converted to composite video. This key signal must undergo a time delay equal to the delay of encoding the digital RGB data into composite video. The four key bits are treated as an unsigned integer equal to the amplitude of the key signal. A zero for the key bits is equivalent to 0 IRE for the key amplitude, while a 15 for the key bits is equivalent to 100 IRE key amplitude.

One bit of cursor (prompt or status) information will have to be added to the composite video signal to generate color edit.

The encoder takes the appropriate signals from the gen-lock source, and color information from the mainframe, and produces the composite video signal in either NTSC, PAL, or PAL-M formats, depending on configuration. While the NTSC and PAL encoders have significant operational differences, the block diagram (Figure 3-11) is sufficient for both, and functional differences will be pointed out as they are encountered.

Three D/A converters (U29, U36, U42) each convert 8 bits of digital color data into analog levels. The converters produce a zero voltage when provided with a zero input, and produce a maximum voltage output when provided with an input of 255. The maximum voltage is a function of the matrix block.

The MATRIX block is a resistive network that is the front end of the Y, U, and V amplifiers. The matrix sums the analog RGB signals according to the standard equations:

$$Y = 0.299R + 0.587G + 0.144B$$

$$U = 0.493(B - Y) = -0.147R - 0.287G + 0.437B$$

$$V = 0.877(R - Y) = 0.615R - 0.515G - 0.100B$$

The MATRIX block also sums burst gate into the U and V channels.

The LUMA AMP (U45) and DELAY (U47, U46) has a fixed delay equal to the delay of the chrominance signals. The delay of the luminance is such that a signal input at R, G, or B will reach its 50% point at the output of the chroma amplifier simultaneously with it reaching its 50% point at the output of the luminance amplifier. The blanking signal is added to the luminance signal to form a pedestal for NTSC.

The NOTCH FILTER (L15, C151) in the Y path attenuates the subcarrier frequency in the luminance path. The center frequency of the notch filter has a 6dB attenuation of the subcarrier frequency (3.58MHz or 4.43MHz, depending on the system configuration). There is a 3dB attenuation 200KHz on either side of the center frequency, and no attenuation at 400KHz on either side. A switch on the Sync Gen front panel (S1 - 2) allows the technician to disable the notch filter, if desired.

For NTSC systems, the frequency response of the circuit is flat (+/- 0.25dB) to 4.2 MHz. For PAL systems the frequency response is flat to 5.5 MHz.

The U amplifier (U32) conditions the U signal for input to the modulator. The U filter (L1, L2) attenuates frequencies above 1.5MHz, corresponding to a response time of about 350ns.

The V amplifier (U39) conditions the V signal for input to the modulator. The V filter (L6, L7) attenuates any frequency above 1.5MHz by at least 6dB, and attenuates any frequency above 2.5MHz by at least 20dB. A front panel switch (S1 - 3) allows the technician to disable the chroma signal from the output for test purposes.

The subcarrier from the gen-lock is processed by a band-pass filter (L3, L4, L5) and sent to the modulator (where it modulates the U signal) and to the 90-degree phase shift network.

The QUADRATURE adjustment section takes the subcarrier and phase shifts (delays) the subcarrier by 90 degrees to generate the V subcarrier. This phase shift must be exactly 90 degrees, and may be adjusted by R221.

In PAL systems, the output of the quadrature adjustment must go to the V-axis inverter. (This block is bypassed on the NTSC encoder board.) This block inverts the subcarrier (shifts it by 180 degrees) on alternate scanlines. This is adjusted using C158, to exactly 180°.

The MODULATOR (U33, U40) section performs a suppressed-carrier balanced modulation of the U and V input signals with the subcarrier inputs.

The output of the modulator is amplified by U34, low-pass filtered through L9 to remove high-order harmonics, and then passed along to the output summing amp.

The SYNC processor (Q46, Q47) conditions the inputs for the output amplifier. Sync has a fall time of 140 ns for NTSC systems and 250 ns for PAL systems. The overall delay of Sync can be adjusted (by J5) to match the delay of R, G, and B from input to output to within 40 ns. This delay is measured at 50% points.

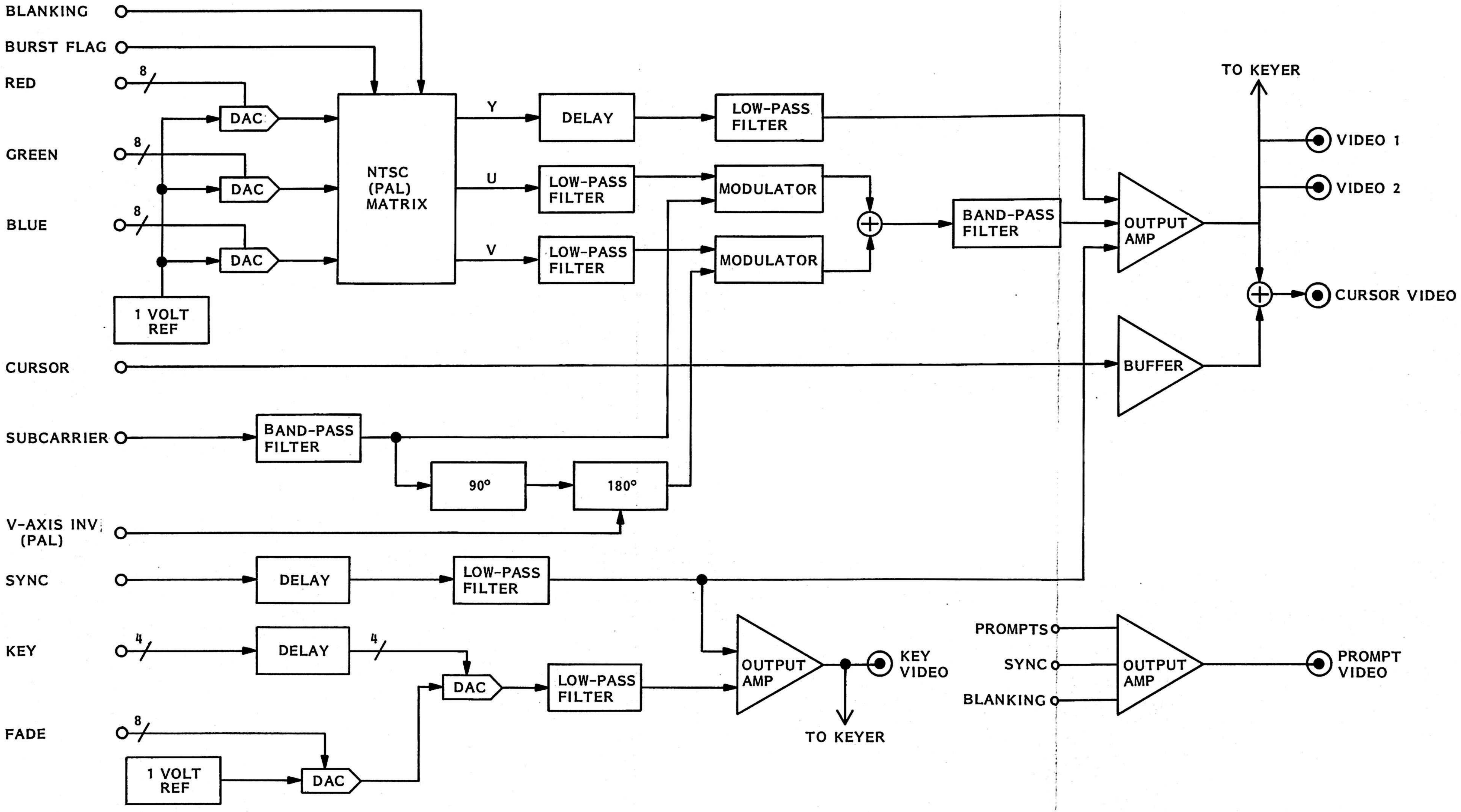

BLANKING
BURST FLAG
RED
8
GREEN
8
BLUE
8
DAC
DAC
DAC
1 VOLT REF
NTSC (PAL) MATRIX
Y
U
V
DELAY
LOW-PASS FILTER
LOW-PASS FILTER
LOW-PASS FILTER
MODULATOR
MODULATOR
BAND-PASS FILTER
OUTPUT AMP
TO KEYER
VIDEO 1
VIDEO 2
CURSOR VIDEO
CURSOR
BUFFER
SUBCARRIER
BAND-PASS FILTER
90°
180°
V-AXIS INV (PAL)
SYNC
DELAY
LOW-PASS FILTER
KEY
4
DELAY
4
DAC
LOW-PASS FILTER
OUTPUT AMP
KEY VIDEO
TO KEYER
FADE
8
1 VOLT REF
DAC
PROMPTS
SYNC
BLANKING
OUTPUT AMP
PROMPT VIDEO

Figure 3-12. Video Encoder Section Block Diagram

The OUTPUT AMP (U51, U52) combines the luminance, chrominance, and sync into a composite video signal capable of driving a 75-ohm cable. The driver is capable of driving four (4) separate 75-ohm cables with no noticable signal loss (less than 1%) and a return loss of less than 40dB. The amplifier and inputs are arranged in such a way that disabling any input has no effect on the output other than removing the desired component.

CURSOR information is added through Q50 and Q49 to the output video to provide a COLOR EDIT output video signal.

3.10.2.1 Inputs from Digital Section.

A) Digital RGB, 8 bits each color, 24 bits total
B) Digital KEY signal, 4 bits
C) Digital cursor signal, 1 bit
D) Digital prompt signal, 1 bit

3.10.2.2 Outputs from Sync Generator Section.

See paragraph 3.10.1.3.

3.10.2.3 Outputs to Customer.

All signals are 1 volt peak-to-peak

A) SCRIBE encoded video (2 outputs), either NTSC, PAL, or PAL-M.
B) RGB video (3 outputs), -4v composite sync on green (OPTIONAL)
C) Key video (1 output), used with RGB option.
D) Color Edit video (1 output), displays SCRIBE video plus cursor.
E) B&W prompts (1 output), displays status and menu information only.
F) DLY KEY (delayed key, 1 output), to be used as the external key on a switcher while keying SCRIBE video.

3.10.2.4 Adjustments Available To Customer. These adjustments are available on the encoder PC board, accessible through the SCRIBE back door:

A) Luminance amplitude of SCRIBE video (+/- 3dB)
B) Chrominance amplitude of SCRIBE video (+/- 3dB)
C) Burst amplitude
D) Sync amplitude

3.10.3 PREVIEW OUTPUT (OPTIONAL)

The preview output option (U54) provides the operator with a low-cost output containing non-antialiased characters plus cursor. This preview output is used as a composition and positioning aid for the operator. Since this is a non-antialiased output it is not to be used for broadcast purposes.

3.10.4 KEYER/FADER (OPTIONAL)

With the internal keyer/fader (Figure 3-13), a customer is able to insert the SCRIBE video over the input video in the same manner as a downstream keyer. The ratio of SCRIBE video to Program video depends on the level of the key signal. Zero IRE for key level means 100% program video, while 100 IRE for key level will mean 100% SCRIBE video.

The Keyer/Fader superimposes the SCRIBE output signal over the Program input by a mixing process. SCRIBE video is attenuated linearly by the KEY signal, and Program Input is attenuated by (1-KEY) signal, then these two signals are added together.

PROGRAM VIDEO is input to a pre-amp (U18) which DC restores it to zero volts at the blanking level.

Eight bits of FADE are input to a D/A converter (U15), which creates a control voltage used to fade the characters on and off the screen.

This voltage is used as the reference voltage to a multiplying D/A converter (U16), whose data inputs are the four KEY bits. The key data represents the "hole" in which characters, edges, and background stripes are to be inserted. The key data is delayed (by U20, U21, U22, U23, and U14) by an amount equal to the delay necessary to encode the composite signal.

The 4-bit digital KEY signal from the mainframe is delayed the same amount of time as the R, G, and B SCRIBE signals are during encoding and converted to an analog signal. A 4-bit D/A converter (U16) converts the digital KEY signal and adds the composite sync signal. This combined signal is input to output amplifier U41. U41 simultaneously drives the output Key Video, the preview mixer, and the program mixer.

There is another control signal Fade Enable which disables the key control signal (by Q37) going to the program mixer. This enables the operator to monitor a page on the preview output without affecting the program output.

Both the preview and the program keyers have line driver outputs, and have DC, luminance, and chrominance gain controls. These controls are accessible through the rear panel.

3.10.4.1 Keyer/Fader Inputs.

a. Program video from Customer (1 volt peak-to-peak)

b. SCRIBE video from encoder

c. KEY00 - KEY03 (TTL compatible)

d. FADE00 - FADE07: This bus controls fading on preview channel. If FADE = 0 then titles are off. If FADE = $FF then titles are full on.

e. FADEEN*: Fade enable signal, which enables keying over program.

3.10.4.2 Keyer/Fader Outputs.

a. Preview Video (1 output): The output will always display SCRIBE over Program.

b. Program Video (2 outputs): This output will display only Program when INSERT is off, and SCRIBE over Program when INSERT is on. One of the outputs has a bypass relay that passes PROGRAM IN to its output when power is removed from the board.

c. Delayed Key (1 output): This output is used for composite output of keyer.

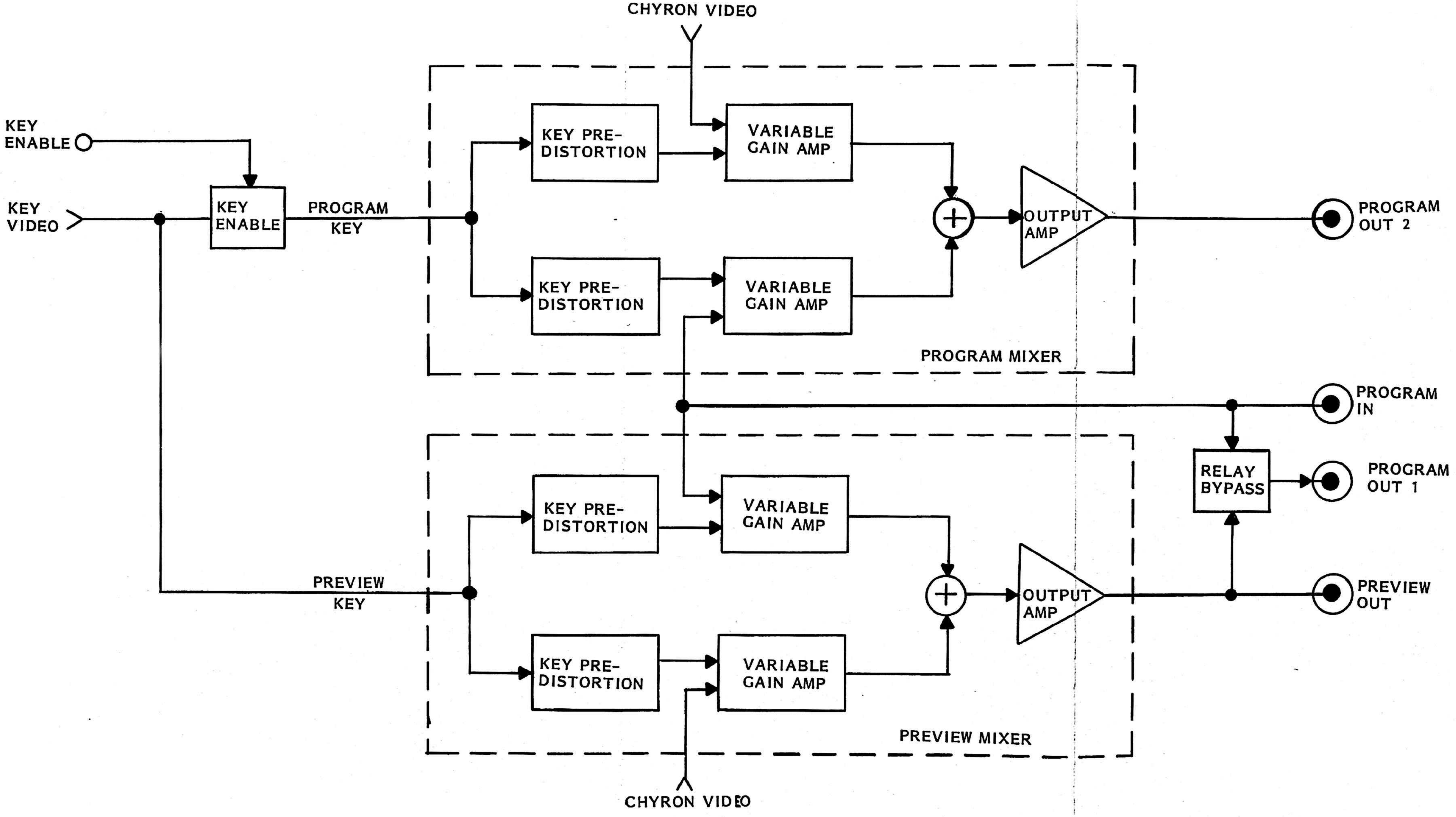

CHYRON VIDEO
KEY ENABLE
KEY VIDEO
KEY ENABLE
PROGRAM KEY
KEY PRE-DISTORTION
VARIABLE GAIN AMP
KEY PRE-DISTORTION
VARIABLE GAIN AMP
OUTPUT AMP
PROGRAM OUT 2
PROGRAM MIXER
PROGRAM IN
RELAY BYPASS
PROGRAM OUT 1
KEY PRE-DISTORTION
VARIABLE GAIN AMP
PREVIEW KEY
OUTPUT AMP
PREVIEW OUT
KEY PRE-DISTORTION
VARIABLE GAIN AMP
PREVIEW MIXER
CHYRON VIDEO

Figure 3-13. Keyer/Fader Functional Block Diagram

Section 4

SCRIBE DIAGNOSTIC OPERATION

4.1 GENERAL

The SCRIBE diagnostic programs allow the technician to test and exercise individual sections of the system, and isolate malfunctions to a board level. Once a malfunction has been isolated to an individual circuit board, the faulty board can be swapped with a working board, and SCRIBE operation can commence with a minimum of downtime.

The technician must become familiar with the functional overview and theory of operation of the SCRIBE system (in Sections 2 and 3 of this manual) before proceeding with the diagnostic programs.

4.1.1 OVERVIEW

The SCRIBE diagnostic programs are organized so that the technician can make a hypothesis about the observed system malfunction, then isolate the difficulty by testing each subsystem that may be involved. The diagnostic programs are constructed to minimize board interaction effects that could cause misdiagnosis.

4.1.1.1 APPROACH

The most effective approach to use when using the diagnostic programs involves observing system operation, making a hypothesis as to the system's malfunction, and finally testing the suspected subsystems to verify proper operation. Usually, you will be able to test a subsystem in more than one way, which allows for efficient troubleshooting and minimizes the possibility of false diagnosis.

For example, if you observe that the system is not rolling displays correctly, you can test the roll function through the Frame Buffer diagnostic programs. The roll function diagnostic does not use the BMPU board, but resets values in the jump table memory to create a roll display. If the roll function operates correctly in this test, yet does not operate normally at a system level, then the BMPU board or the VMX (frame buffer) interface might be causing the trouble.

4.1.1.2 Capabilities/Limitations The SCRIBE diagnostic programs can be used to isolate system malfunctions to a circuit board level. Although the program can point out "suspect" chips, other factors (such as address latch failures, RAS*/CAS* signal failures, etc.) can cause chips to show up as suspect. In general, the malfunctioning circuit board should be swapped with a known working board to restore SCRIBE operation. Since isolating malfunctions on individual circuit boards requires specialized test fixtures and procedures not available at standard test facilities, such troubleshooting will be performed at the CHYRON factory.

Refer to paragraph 4.10 for general disassembly instructions. Refer to paragraph 4.11 for instructions on how to obtain assistance, or how to obtain replacement circuit boards.

4.1.2 EQUIPMENT REQUIRED

The following equipment is required to operate the SCRIBE diagnostic programs:

- SCRIBE Diagnostic Programs Diskette
- Digital Voltmeter with probes
- RS-232C Terminal with Keyboard, configured for Full Duplex operation, 9600 baud. (terminal is optional; used when keyboard/transition board subsystems are not operating properly)
- Waveform Monitor

4.1.3 DIAGNOSTIC PROGRAM MENU OPERATION

The SCRIBE diagnostic programs operate using a menu operating system which allows you to proceed through tests on a block by block basis. Starting from one of the eight diagnostic test groups (listed in paragraph 4.1.4), you can proceed through groups of subtests until you have either verified subsystem operation or have isolated a malfunction.

Menu choices appear on the Prompts monitor, and selections are made by using the SCRIBE keyboard. In some tests, you will observe the Program Out display on a color monitor to verify operation of a subsystem.

If for any reason the Prompts display or the keyboard/transition board subsystems are not functioning, you can use a CRT terminal and the SCRIBE's RS-232 port to run the diagnostics. Instructions for configuring the CRT terminal appear in paragraph 4.1.3.2.

4.1.3.1 **Getting Started** The SCRIBE diagnostics are diskette based. Therefore, the disk subsystems (disk drive and disk controller) have to be functioning to load the system diagnostic programs.

To run the SCRIBE diagnostics programs, first power down the SCRIBE system. Then, load the SCRIBE diagnostics diskette into a floppy disk drive, and power up the system. The system will complete its power-up diagnostics, then it will respond with the Diagnostics Program Initial Menu (Figure 4-1):

```
SCRIBE OPERATING SYSTEM        1.00

          B . . . .  REBOOT SYSTEM
          R . . . .  RESTART PROGRAM
          D . . . .  DIAGNOSTICS
```

Figure 4-1. SCRIBE Diagnostic Programs Initial Menu

To start the diagnostic program, enter "D" on the keyboard, then press NEWLINE.

Once the program has loaded from the diagnostics diskette, the system will respond with the Diagnostics Subtests Menu (Figure 4-2):

```
    * * *   SCRIBE DIAGNOSTICS   * * *

1.  DISPLAY & CURSOR
2.  FRAME BUFFER
3.  BITSLICE
4.  FONT MEMORY
5.  CPU
6.  KEYBOARD
7.  TRANSITION BOARD
```

Figure 4-2. Diagnostics Subtests Menu

Choose the test desired by entering its number on the SCRIBE keyboard.

4.1.3.2 Configuring CRT Terminal for Diagnostic Operation

The CRT terminal must use the RS-232 protocol to communicate with the SCRIBE system. The terminal connects to the DB-25 connector on the MVME117 CPU board. The SCRIBE system is considered DCE for hook-up purposes. To configure the CRT terminal for diagnostic operation, use these specifications:

- 9600 baud
- 8 data bits
- 1 stop bit
- no parity bits

If you have any difficulty configuring your terminal for SCRIBE diagnostics operation, please contact CHYRON Customer Service for assistance.

4.1.4 MAJOR DIAGNOSTIC TEST GROUPS

There are eight major diagnostic test groups, each of which has up to eight subtests. Each major subgroup is described in detail in a separate paragraph, which is listed below. The major test groups are:

Major Diagnostic Test Group	Paragraph
Display and Cursor Diagnostics	4.2
Frame Buffer Diagnostics	4.3
Bitslice (BMPU) Diagnostics	4.4
Font Memory Diagnostics	4.5
CPU Diagnostics	4.6
Keyboard Diagnostics	4.7
Transition Board Diagnostics	4.8

4.1.4.1 **Display and Cursor Diagnostic Group Overview** The display and cursor diagnostics test the display and cursor subsystems of the SCRIBE. These tests verify proper operation or isolate malfunctions to these subsystems:

- VME interface
- CRT controller circuitry
- cursor, tabs, safetitle memory
- background palette memory
- character palettes memory
- anti-alias circuitry
- fade latch circuitry

4.1.4.2 **Frame Buffer Diagnostic Group** The frame buffer diagnostics test the frame buffer subsystems of the SCRIBE. These tests verify proper operation or isolate malfunctions to these subsystems:

- memory and address decoding logic
- VME/VMX interfaces
- anti-alias circuitry
- erase logic
- crawl hardware
- roll hardware
- video RAM refresh logic

4.1.4.3 **Bitslice (BMPU) Diagnostic Group** The bitslice (BMPU) diagnostics test the bitslice (BMPU) board and related circuitry. These tests verify proper operation or isolate faults to these subsystems:

- VME interface
- VMX (font memory) interface
- VMX (frame buffer) interface
- WCS RAM circuitry
- map RAM circuitry
- operational logic (timing, etc.)

4.1.4.4 **Font Memory Diagnostic Group Overview** The font memory diagnostics test the font memory and related subsystems of the SCRIBE. These tests verify proper operation or isolate malfunctions to these subsystems:

- VME interface
- VMX (font memory - BMPU) interface
- parity interrupt logic
- font memory RAM locations
- address decoding logic
- refresh logic
- BMPU/VME simultaneous access logic

4.1.4.5 **CPU Circuitry Diagnostic Group Overview** The CPU circuitry diagnostics test the CPU board and related circuitry. These tests verify proper operation or isolate faults to these subsystems:

- 68010 MPU
- ROM
- RAM (parity disabled)
- Parity Logic
- Parity RAM
- RAM (parity enabled)
- CMOS RAM
- Serial Port Logic
- PTM Logic
- Real-Time Clock Logic
- 68881 (co-processor)
- SCSI Logic
- Abort Logic
- Fail LED Logic

4.1.4.6 Keyboard Subsystems Diagnostic Overview The keyboard subsystems diagnostics test the keyboard and related subsystems of the SCRIBE. These tests verify proper operation or isolate malfunctions to these subsystems:

- ASCII/Functional Description Test
- Keyboard Interrupts Test

4.1.4.8 Transition Board Diagnostic Group Overview The transition board diagnostics test the transition board and related circuitry of the SCRIBE. These tests verify proper operation or isolate malfunctions to these circuits:

- DCD Interrupt (S1) Test
- CTS Interrupt (S2) Test

4.1.5 DIAGNOSTICS ERROR LOG

The diagnostics error log contains a record of all failures while running a particular diagnostic program. Thus, if you are operating the Frame Buffer tests, and the test encounters an error, the error log records the suspected chip number(s), the number of failures, and the addresses where the failures occurred.

The information contained in the error log is useful for isolating failures in the Frame Buffer and Font Memory subsystems. This information is especially useful to our Customer Service engineers, who will need to know exactly what is contained in the error log before recommending a course of action for repair.

Please note that any chip that is listed as "suspect" in the error log may not be faulty. There are many other reasons that a chip can show up as suspect- failures generally happen in patterns, and from the pattern, the type of failure (and course of repair action) can be determined.

After an error is encountered, the system will respond with:

"**Output Error Log? ENTER Y or N**"

If you enter "Y" here, the system will output the contents of the error log. In some cases, the system will display the suspected chip number(s), and then will ask if you want to output the error log (which would contain the number of failures and the addresses of the failures).

The error log will record up to 100 (hex) errors per memory chip, and will record up to 50 addresses with errors.

NOTE: If an error log file for a particular test extends over one page, the system will prompt for a carriage-return [<CR> or NEWLINE] before displaying the next page.

4.2 DISPLAY AND CURSOR DIAGNOSTICS

4.2.1 GENERAL

This paragraph describes the display and cursor diagnostics for the SCRIBE system. This paragraph includes a complete listing of all applicable subtests, operating instructions for the diagnostic programs, and instructions for how to interpret the results of each subtest.

4.2.2 DESCRIPTIONS OF SUBTESTS

Table 4-1 contains a list of subtests associated with the display and cursor diagnostic programs, as well as a brief description for each.

Table 4-1. Display and Cursor Diagnostics Subtests

Subtest name	Description
VME Interface Diagnostics	Tests the VME interface between the display and cursor board and the CPU board.
CRT Controller Diagnostics	Tests the CRT controller subsection by displaying test messages to the Prompts monitor.
Cursor, Tabs, Safetitle Memory Diagnostics	Tests the cursor, tabs, and safe title functions, as well as their memory circuitry. Also tests tab and safe title marker operation.
Background Palette Diagnostics	This test writes to the background palette, and queries the technician as to the color and quality of the written background, which appears on the Program Out outputs.
Character Palette Diagnostics	This program tests the character palette memory through write/reads, and also tests the palette/ alternate palette memory.
Anti-Alias Diagnostics	The anti-alias diagnostics test the primary/mix logic by providing a visual display of anti-alias values. Errors show up as visible anomalies.

Table 4-1. Display and Cursor Diagnostics Subtests, continued

Subtest name	Description
Fade Latch diagnostics	Tests the fade latch logic by fading a display as the value of the fade latch is changed.
Key Test	Tests the key/mix logic by testing for key/mix locations on the Display and Cursor board.

4.2.3 OPERATIONAL INSTRUCTIONS

This paragraph contains operational instructions for how to operate the display and cursor diagnostic programs, which are listed and described in paragraph 4.2.2.

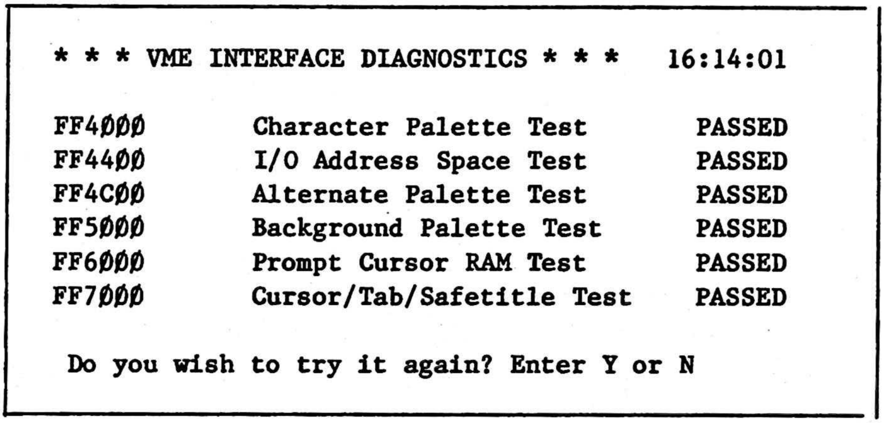
4.2.3.1 **VME Interface Diagnostics** These diagnostic programs test the following subsystems of the VME interface by looking for DTACK*:

- Character Palette
- I/O Address Space
- Alternate Palette
- Background Palette
- Prompt Monitor RAM
- Cursor/Tab/Safetitle Logic

To run these tests, use the following procedure.

Step 1: From the Display & Cursor diagnostics menu, select the VME Interface Diagnostics be entering "1" from the SCRIBE A/N keyboard.

The diagnostic subroutines will test the associated circuitry, and post the results as shown in Figure 4-3.



```
* * * VME INTERFACE DIAGNOSTICS * * *     16:14:01

FF40000        Character Palette Test        PASSED
FF44000        I/O Address Space Test        PASSED
FF4C000        Alternate Palette Test        PASSED
FF50000        Background Palette Test       PASSED
FF60000        Prompt Cursor RAM Test        PASSED
FF70000        Cursor/Tab/Safetitle Test     PASSED

 Do you wish to try it again? Enter Y or N
```

Figure 4-3. VME Interface Diagnostic Display

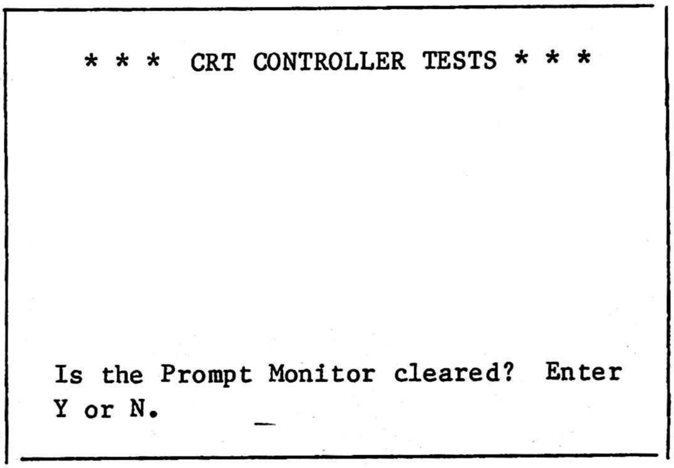
If all VME interface subsystems pass the test, proceed with diagnostic operation elsewhere. If a subsystem fails, run the tests again. If a subsystem keeps failing, then that subsystem on the Display & Cursor board has failed. Replace the Display & Cursor board.

Step 2: Enter Y to run the VME diagnostic subroutines again. Enter N to return to the Display & Cursor main menu.

4.2.3.2 **CRT Controller Diagnostics** The CRT controller diagnostics test the prompt monitor display logic and allow alignment of the prompt monitor's borders.

To run these these diagnostics, use the following procedure.

Step 1: From the Display & Cursor Diagnostics main menu, select "2" for CRT controller diagnostics. The system will respond with Figure 4-4, below:



```
     * * *  CRT CONTROLLER TESTS * * *









Is the Prompt Monitor cleared?  Enter
Y or N.       _
```

Figure 4-4. CRT Controller Tests Menu #1

Step 2: If the entire prompt monitor is cleared except for the title and the prompt on the bottom of the screen, respond with "Y" and proceed to Step 4. If not, respond with "N".

Step 3: If the prompt monitor did <u>not</u> clear during the test and you responded with "N", the system will respond with:

Do you want to try it again? Enter Y or N

To run the test again, enter Y. To leave the CRT controller diagnostics, enter "N".

Step 4: If the CRT Controller passes the clear-monitor test in Steps 1 and 2, the system will proceed with the filled-monitor test as shown in Figure 4-5:

```
      * * *  CRT CONTROLLER TESTS * * *








   Is the Prompt Monitor Filled?   Enter
   Y or N.
```

Figure 4-5. CRT Controller Tests Menu #2

Step 5: If the entire prompt monitor is filled except for the prompt on the bottom of the screen, respond with "Y" and proceed to Step 7. If not, respond with "N".

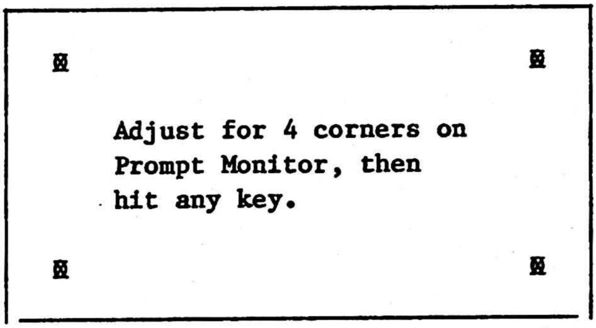
Step 6: If the prompt monitor did not fill during the test and you responded with "N", the system will respond with:

Do you want to try it again? Enter Y or N

To run the test again, enter Y. To leave the CRT controller diagnostics, enter "N".

Step 7: If the CRT controller passed the filled-monitor test in Steps 4 and 5, the system will proceed with the prompt monitor alignment (Figure 4-6).

NOTE: This procedure requires the use of the card-case extender board in the SCRIBE mainframe. Potentiometer R1 on the Display & Cursor Board is not accessible without the extender board.



⊠ ⊠

Adjust for 4 corners on
Prompt Monitor, then
hit any key.

⊠ ⊠

Figure 4-6. CRT Controller Diagnostics Menu #3

Step 8: If an adjustment is necessary, power down the SCRIBE, remove the Display & Cursor Board from the card cage, insert the extender board, and install the Display & Cursor Board into the extender board.

Power up the SCRIBE, and re-boot the diagnostics to proceed.

Use R1 on the Analog Board (located on the Display & Cursor Board, near the upper outside corner) to adjust the markers so that they reside in the four corners of the prompt monitor.

Step 9: Press any key when done. This concludes the CRT Controller diagnostics, and you return to the Display & Cursor main menu.

4.2.3.3 Cursor/Tab/Safetitle Diagnostics The cursor/tab/safetitle diagnostics test the memory locations on the Display & Cursor board that control the cursor, tab, and safe title functions. Also, these diagnostics provide a means of testing each function individually, from an operational standpoint.

To operate the cursor/tab/safetitle diagnostics, follow this procedure.

Step 1: From the Display & Cursor Diagnostics main menu, enter "3" to run the cursor/tab/safetitle tests. The system will respond with Figure 4-7:

```
Cursor/Tab/Safetitle Tests 8:01:23

Cursor/Tab/Safetitle Memory PASSED

Cursor Diagnostics:

Use direction arrows to move
cursor.  Enter value to LEDs.

Hit ESC to exit to next test.
```

Figure 4-7. Cursor/Tabs/Safetitle Tests Menu #1

Step 2: Enter a value on the address keypad as an increment for cursor movement.

Step 3: Observe Program Out on a monitor. Using the cursor direction keys, move the cursor on the Program Out screen. If the cursor does not move as it should, the cursor logic may be faulty.. Continue with testing to isolate the difficulty.

Step 4: When you are satisfied with cursor logic performance as tested in Step 3, press the ESC key. The system will then test the tab logic.

Step 5: After you press the ESC key, the following display (Figure 4-8) will appear on the Prompts monitor.

```
Cursor/Tab/Safetitle Tests 8:51:21

Cursor/tab/safetitle memory PASSED

Safetitle Diagnostics:

Use direction arrows to move
safetitle.  Enter value to LEDs

      T = Top safetitle
      B = Bottom safetitle
      R = Right safetitle
      L = Left safetitle

Hit ESC to exit to next test
```

Figure 4-8. Cursor/Tabs/Safetitle Tests Menu #2

Step 6: Enter an increment value on the address keypad. Check the Address LEDs to verify the value as entered.

Step 7: Observe the Cursor Out channel on a monitor. Choose the safetitle marker to be moved by pressing one of the T, B, R, or L keys.

Step 8: Using the cursor direction keys, move the selected marker on the Cursor Out screen.

Step 9: Perform Steps 7 and 8 with each safetitle marker. If any marker does not move correctly, the safetitle logic on the Display & Cursor board may be faulty. Continue with testing to isolate the difficulty more accurately.

Step 10: After you are satisfied with safetitle operation, press the ESC key to proceed to the TAB logic test. The following display (Figure 4-9) will appear on the Prompt monitor:

```
Cursor/tab/safetitle tests 8:59:01

Cursor/Tab/safetitle memory PASSED

Tab Diagnostics:

Move cursor using arrows & LEDs,
use tabkey to set tabs.
Use SHIFT TAB to remove tabs.

Hit ESC to exit to next test.
```

Figure 4-9. Cursor/Tabs/Safetitle Tests Menu #3

Step 11: Enter an increment value on the address keypad. observe the Cursor Out channel for cursor and tab displays.

Step 12: Using the cursor direction keys, move the cursor on the screen. Use the TAB key to place tabs. Use the SHIFT-TAB combination to remove tabs settings.

Step 13: After you've verified tab logic operation, press ESC to exit. This concludes the Cursor/Tab/ Safetitle Diagnostics, and the SCRIBE returns to the Display & Cursor main menu.

4.2.3.4 Background Palette Diagnostics This series of tests verifies operation of the background palette logic on the Display & Cursor board. Follow this procedure to complete these tests.

Step 1: From the Display & Cursor main menu, enter "4" to begin the background palette tests. The system will respond with the following display (Figure 4-10):

```
        BACKGROUND PALETTE DIAGNOSTICS

   Background palette memory test  PASSED

   (please stand by for visual test)

                 then...

   Is the screen black?  Enter Y or N
```

Figure 4-10. Background Palette Diagnostics Menu #1

Step 2: Observe the Cursor Out channel. If the background is black, enter "Y", and proceed to Step 3. If the background is not black, enter "N". The system will respond with:

```
Do you wish to try it again?  Enter Y or N
```

If you enter "Y" after this prompt, the test will repeat. If the screen still will not clear to black, then the background palette logic on the Display & Cursor board is faulty, and the board must be replaced.

If you enter "N" here, the system will return to the Display & Cursor main menu.

Step 3: After the "black" background test, the system will prompt with:

Is the screen blue? Enter Y or N

A graduated blue background (darker on top) should appear on the program output. If this is the case, enter "Y" and proceed to Step 4. If this is not the case, repeat the test (as shown in Step 2) until good/bad operation is verified.

Step 4: After the "blue" background test, the system will prompt with:

Is the screen red? Enter Y or N

A graduated red background (darker on top) should appear on the program output. If this is the case, enter "Y" and proceed to Step 5. If this is not the case, repeat the test (as shown in Step 2) until good/bad operation is verified.

Step 5: After the "red" background test, the system will prompt with:

Is the screen green? Enter Y or N

A graduated green background (darker on top) should appear on the program output. If this is the case, enter "Y" and proceed to Step 6. If this is not the case, repeat the test (as shown in Step 2) until good/bad operation is verified.

Step 6: After the "green" background test, the system will prompt with:

Is program video seen on all scan lines? Enter Y or N

In this test, the background palette is set to "clear", allowing program input to be displayed on the program output. If program video _is_ visible on all scan lines, enter "Y".

If this is _not_ the case, repeat the test (as shown in Step 2) until you've verified good or bad operation. If operation is _not_ restored, the background palette logic is faulty, and the Display & Cursor board must be replaced.

Step 7: After the conclusion of Step 6, the system will prompt with:

Do you want to run this test again? Enter Y or N

If you enter "N" here, the system goes back to the Display & Cursor main menu.

If you enter "Y" here, the system will repeat the Background Palette diagnostics from the top (Step 1).

4.2.3.5 _Character Palettes Diagnostics_ The character palettes diagnostics test the two character palette memories by displaying colored boxes from both palettes, and having the technician discern any differences. Such a difference would indicate a malfunction of the character palette.

To run these tests, follow this procedure:

Step 1: From the Display & Cursor main menu, select "5" to call up the Character Palettes Diagnostics. The following display (Figure 4-11) will appear on the Prompt Monitor.

```
Character Palettes Diagnostics  6:42:11

Character Palette #1 Memory Test  PASSED
Character Palette #2 Memory Test  PASSED

 Compare top color box (palette 0) to
 bottom color box (palette 1)

 Are both boxes green?  Enter Y or N

 Hit ESC to exit to next test
```

Figure 4-11. Character Palette Diagnostics Menu #1

Step 2: Observe the program output on a color monitor. There should be two green boxes, one over the other, on the color monitor. If this is not the case, then there is a malfunction in the character palette logic. Go on to Step 3. If this is the case, enter "Y" and go on to Step 4.

Step 3: If the color boxes do not appear as the same color, or if only one box appears on the output, then there is a problem with the character palette memory. Enter "N". The system will prompt with:

Do you wish to try it again? Enter Y or N

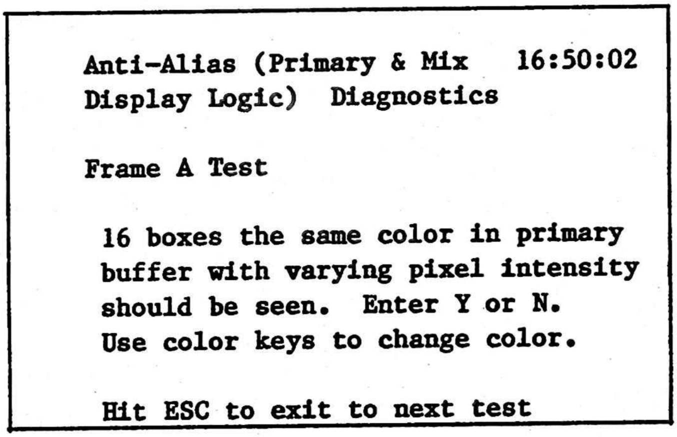
If you enter "Y" here, the test will restart. If you enter "N", the system returns to the Display & Cursor main menu.

Step 4: If the green color boxes appeared correctly and you entered "Y" to the system's prompt, the system will continue testing with blue boxes, then cyan, red, yellow, magenta, white, and black. Follow the procedure in Steps 2 and 3 for each new color. If any of the colors consistently appear wrong, then that indicates a malfunction with the character palette memory or logic. When the test is complete, press the ESC key to exit.

4.2.3.6 Anti-Alias Diagnostics The SCRIBE anti-alias diagnostics test the primary and mix display logic by displaying 16 boxes from each frame buffer of the same color, with 16 different display intensities. The technician should look at each display, and try to discern any abnormality, which would indicate a malfunction.

To run the anti-alias diagnostics, follow this procedure:

Step 1: From the Display & Cursor main menu, enter "6". The system will respond with Figure 4-12:



```
Anti-Alias (Primary & Mix   16:50:02
Display Logic)  Diagnostics

Frame A Test

 16 boxes the same color in primary
 buffer with varying pixel intensity
 should be seen.  Enter Y or N.
 Use color keys to change color.

 Hit ESC to exit to next test
```

Figure 4-12. Anti-Alias Diagnostics Menu #1

Step 2: Observe the COLOR EDIT output and look for anomalies such as blank (missing) boxes, or incorrect intensities. If the boxes are displayed incorrectly, there may be a malfunction in Frame Buffer A anti-alias logic.

Step 3: Use the color keys on the SCRIBE keyboard to change colors on the screen. After each change in color, examine the COLOR EDIT display for problems.

Step 4: After you've examined the display with all eight colors, enter "Y" to go on to the next test. (If there is a problem with any display, enter "N" here, and the Frame A Test will repeat, allowing you to further examine the malfunction.

Step 5: After the Frame A pixel-intensity test has been completed and you've entered "Y", the system will respond with Figure 4-13 "A".

```
Anti-Alias (Primary & Mix    16:54:02
Display Logic) Diagnostics

Frame A Test

 Are any boxes seen?

 Enter Y or N.
 Hit ESC to exit to next test.
```

Figure 4-13 "A". Anti-Alias Diagnostics Menu #2

Step 6: Observe the COLOR EDIT output and look for any boxes on the display. If any boxes appear, there may be a malfunction with the Frame A anti-alias logic.

Step 7: If there are no boxes visible on the COLOR EDIT output, enter "N" to go on to the next test. (If there is a problem with the display, enter "Y" here, and the Frame A Test will repeat, allowing you to further examine the malfunction.)

Step 8: After the Frame A anit-alias level test has been completed and you've entered "N", the system will respond with Figure 4-13 "B".

```
Anti-Alias (Primary & Mix   16:57:07
Display Logic) Diagnostics

Frame A Test

16 Boxes in mix buffer of varying
intensity should be seen, but with
primary intensity = F.  Enter Y or
N.  Use color keys to change color.

Hit ESC to exit to next test.
```

Figure 4-13 "B". Anti-Alias Diagnostics Menu #3

Step 9: Observe the COLOR EDIT output and look for anomalies such as blank (missing) boxes, or incorrect levels.

Step 10: If you entered "Y" in Step 9, the system will go on to the Frame B tests, which are identical to the Frame A tests. Go bakc to Step 2 and follow the same procedures used for Frame A to test Frame B.

Step 11: After the Frame B tests are completed, the system will prompt with:

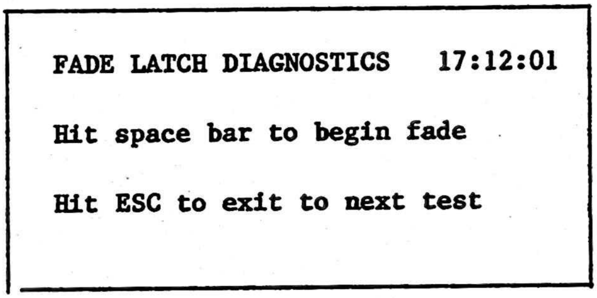
Do you wish to try it again? Enter Y or N

To run the entire diagnostic again, enter Y. To return to the Display & Cursor main menu, enter N.

4.2.3.7 Fade Latch Diagnostics The Fade Latch diagnostics allow you to test for proper operation of the Fade Latch logic on the Display and Cursor board. The Fade Latch logic controls the mix of program video with SCRIBE video during internal keying operations.

To operate the Fade Latch diagnostics, you must connect a valid program video input to PROGRAM IN on the SCRIBE rear panel.

Step 1: From the Display & Cursor main menu, enter "7" to start the Fade Latch diagnostics. The system will respond with Figure 4-14:



```
FADE LATCH DIAGNOSTICS    17:12:01

Hit space bar to begin fade

Hit ESC to exit to next test
```

Figure 4-14. Fade Latch Diagnostics Menu #1

Step 2: Observe the PROGRAM 1 OUT channel on a monitor. Press the space bar to begin the fade. After few seconds, the program video signal should be visible on the display. The following prompt will then appear on the Prompts monitor:

Is program video fully visible? Enter Y or N

If program video is fully visible, enter "Y" here. If program video is not fully visible, enter "N" here. The system will prompt with:

Do you wish to run this test again? Enter Y or N

If you enter "Y" here, the test will restart. If you enter "N" here, the system will return to the Display & Cursor main menu.

Step 3: After the SCRIBE-to-program fade has been executed properly and been acknowledged, the system will respond with Figure 4-15:

```
FADE LATCH DIAGNOSTICS    17:12:01

Hit space bar to begin fade

Hit ESC to exit to next test
```

Figure 4-15. Fade Latch Diagnostics Menu #2

Step 4: Observe the PROGRAM 1 OUT channel on a monitor. Press the space bar to begin the fade. After few seconds, the SCRIBE video signal should be visible on the display. The following prompt will then appear on the Prompts monitor:

Is SCRIBE video fully visible? Enter Y or N

If SCRIBE video is fully visible, enter "Y" here, and the system will return to the Display & Cursor main menu. If SCRIBE video is not fully visible, enter "N" here. The system will prompt with:

Do you wish to run this test again? Enter Y or N

If you enter "Y" here, the test will restart. If you enter "N" here, the system will return to the Display & Cursor main menu.

NOTE: Any failure in the fade latch diagnostics indicates a problem on the Display & Cursor board. If such a problem occurs repeatedly, the Display & Cursor board is faulty and must be replaced.

4.2.3.8 Key Diagnostics This test verifies operation of the keyer/fader logic on the Display & Cursor board. Follow this procedure to complete this test.

Step 1: Connect a source of program video to the PROGRAM IN channel on the SCRIBE rear panel. A color bar display is preferable for this test.

Step 2: From the Display & Cursor main menu, enter "8" to run the Key Test. The system will respond with the following display (Figure 4-16):

```
                KEY DIAGNOSTICS

(please stand by for visual test)

                    then...

Enter Fade Level desired ($00 - FF)
Then <CR>:

Hit ESC to exit to next test
```

Figure 4-16. Key Diagnostics Menu #1

Step 3: Observe the display on the PROGRAM 1 OUT channel. The screen will display a split screen with program video on the top half, and a SCRIBE display with anti-alias mix levels extending over entire screen.

Step 4: Enter the desired fade level (between 00 and FF hex), then press the NEWLINE or <CR> keys. (NOTE: You must enter both digits of the fade value for them to be displayed on the Prompts monitor. The fade will not take place until you press the <CR> or NEWLINE key.)

Step 5: After you enter the desired fade level, you will see the fade level change on the SCRIBE program output. The hex fade value 00 allows all SCRIBE video to show, and the hex fade value FF makes all SCRIBE video transparent. Test all fade values to verify key logic operation.

Step 6: When completed, exit this test by pressing the ESC key. The system will return to the Display & Cursor Diagnostics main menu.

4.3 FRAME BUFFER DIAGNOSTICS

4.3.1 GENERAL

This paragraph describes the frame buffer diagnostics for the SCRIBE system. This paragraph includes a complete listing of all applicable subtests, operating instructions for the diagnostic programs, and instructions for how to interpret the results of each subtest.

4.3.2 DESCRIPTIONS OF SUBTESTS

Table 4-2 contains a list of subtests associated with the frame buffer diagnostic programs, as well as a brief description for each.

Table 4-2. Frame Buffer Diagnostics Subtests

Subtest name	Description
Memory and Address Decode Diagnostics	Tests all frame buffer RAM, using write/reads and checks address decoding.
VME/VMX Interface Diagnostics	Tests the VME/VMX interface by writing to the frame buffer with the BMPU, over the VMX bus and reading the frame buffer with the CPU over the VME bus.

Table 4-2. Frame Buffer Diagnostics Subtests, continued

Subtest name	Description
Anti-Alias Diagnostics	This is a visual test of the primary and mix buffers. This test is done twice, for both Frame A and Frame B. (This test is identical to the Anti-Alias test in the Display & Cursor diagnostics.
Erase Logic Diagnostics	This test fills the frames buffers with FF then issue an erase command to the BMPU. The erase operation should be visible on the screen. The test also checks the frame buffers for 0's after the erase command.
CRAWL Diagnostics	Tests the CRAWL logic by issuing crawl commands (with variable speeds) and having the technician observe the COLOR EDIT or PROGRAM OUT displays for proper operation.
Jump Table Diagnostics	This test decodes addresses of the jump table RAM, and performs a memory test.

Table 4-2. Frame Buffer Diagnostics Subtests, continued

Subtest name	Description
ROLL Diagnostics	This test uses a non-BMPU roll subroutine to roll a test message at variable speed. The test reads a message from disk, displays it, then changes jump table values to roll the message. The BMPU is _not_ used to roll the message.
Refresh Diagnostics	This test displays characters on the program outputs, which are examined for 30 seconds. If no changes occur, the refresh logic is functional.

4.3.3 OPERATIONAL INSTRUCTIONS

This paragraph contains operational instructions for how to operate the frame buffer diagnostics, which are listed and described in paragraph 4.3.2.

4.3.3.1 Memory and Address Decode Diagnostics The memory and address decode diagnostics allow you to test the frame buffers (A, B, C, and D) either one at a time or all at once. To operate these tests, follow this procedure:

Step 1: From the Frame Buffer Diagnostics main menu (#2 from the SCRIBE DIAGNOSTICS menu), enter "1" to select Memory and Address Decode Diagnostics. The system will respond with Figure 4-17:

```
MEMORY & ADDRESS              17:14:01
DECODE DIAGNOSTICS

 Select:
  [1]  FRAME BUFFER A
  [2]  FRAME BUFFER B
  [3]  FRAME BUFFER C
  [4]  FRAME BUFFER D
  [5]  ALL FRAME BUFFERS

  Hit ESC to exit to next test
```

Figure 4-17. Memory & Address Decode Diagnostics Menu #1

Step 2: Select the frame buffer(s) to be tested by entering the appropriate number on the SCRIBE keyboard. The system will begin the test, and will respond with the following message, along with a "bouncing dot" to indicate that the test is in progress.

```
FRAME BUFFER A MEMORY . . . . . . .
```

After the test(s) is (are) completed, the system will respond with:

```
FRAME BUFFER A MEMORY . . . . . . . PASSED
```

If a frame buffer does not pass this test repeatedly, that frame buffer is faulty and must be replaced. (Refer to paragraph 4.1.5, Error Logging, for more information about failures.)

CAUTION

Any failure that specifies a chip as being "SUSPECT" should be treated with caution. Many factors can cause an otherwise good chip to appear faulty, so the pattern of failures provides a clue to the actual failure. When such a failure occurrs, contact CHYRON Customer Service or your Field Representative immediately. Do NOT attempt to replace a chip without assistance from CHYRON Customer Service as this will void your system's warranty!

Step 3: If desired, test the other frame buffers by using the procedure described in Steps 1 and 2.

Step 4: To exit from this test, press the ESC key. The system will return to the Frame Buffer Diagnostics main menu.

4.3.3.2 VME/VMX Interface Diagnostics These tests operate by having the BMPU write/read the frame buffer over the VMX bus, and having the CPU read the data for accuracy over the VME bus. To run the tests, follow this procedure:

Step 1: From the Frame Buffer Diagnostics main menu, select "2" to start the VMX/VME interface diagnostics. The system will respond with Figure 4-18.

```
VMX/VME DIAGNOSTICS        17:24:07

sending WCS to BMPU
   WCS RAM LOADED OK
sending map to BMPU
   MAP RAM DATA LOADED OK
starting BMPU

    VME INTERFACE OK
    VMX INTERFACE OK

   Do you wish to run this
   test again? ENTER Y or N
```

Figure 4-18. VME/VMX Interface Diagnostics Menu #1

Step 2: If the VME and VMX interfaces both tested OK, enter "N", and the system returns to the Frame Buffer Diagnostics main menu. However, if either or both of the interfaces do not pass, enter "Y" here to run the tests again.

If one or both interfaces consistently fail this test, continue testing to isolate the difficulty to the BMPU, the CPU, or to the interface(s).

4.3.3.3 Anti-Alias Diagnostics The SCRIBE anti-alias diagnostics test the primary and mix display logic by displaying 16 boxes from each frame buffer of the same color, with 16 different display intensities. The technician should look at each display, and try to discern any abnormality, which would indicate a malfunction.

To run the anti-alias diagnostics, follow this procedure:

Step 1: From the Frame Buffer Diagnostics main menu, enter "3". The system will respond with Figure 4-19:

```
Anti-Alias (Primary & Mix    17:38:12
Display Logic)  Diagnostics

Frame A Test

 16 boxes the same color in primary
 buffer with varying pixel intensity
 should be seen.  Enter Y or N.
 Use color keys to change color.

 Hit ESC to exit to next test
```

Figure 4-19. Anti-Alias Diagnostics Menu #1

Step 2: Observe the COLOR EDIT output and look for anomalies such as blank (missing) boxes, or incorrect intensities. If the boxes are displayed incorrectly, there may be a malfunction in Frame Buffer A anti-alias logic.

Step 3: Use the color keys on the SCRIBE keyboard to change the colors on the screen. After each change in color, examine the COLOR EDIT display.

Step 4: After you've examined the display with all eight colors, enter "Y" to go on to the next test. (If there is a problem with any display, enter "N" here, and the Frame A Test will repeat, allowing you to further examine the malfunction.

Step 5: After the Frame A pixel-intensity test has been completed and you've entered "Y", the system will respond with Figure 4-20 "A".

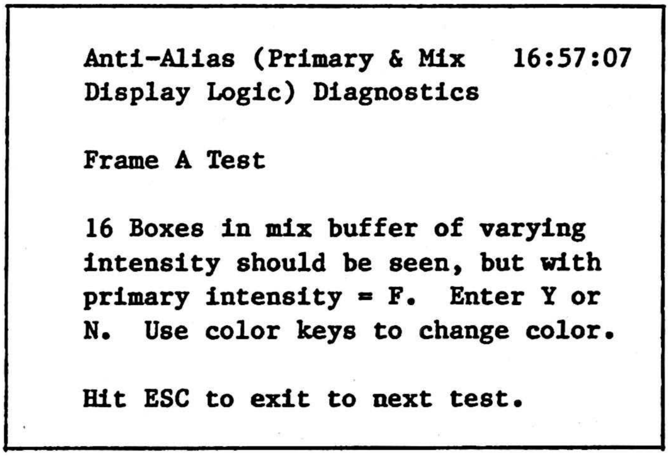
```
Anti-Alias (Primary & Mix   17:54:24
Display Logic)  Diagnostics

Frame A Test

 Are any boxes seen?

 Enter Y or N.
 Hit ESC to exit to next test.
```

Figure 4-20 "A". Anti-Alias Diagnostics Menu #2

Step 6: Observe the COLOR EDIT output and look for any boxes on the display. If any boxes appear, there may be a malfunction with the Frame A erase logic.

Step 7: If there are no boxes visible on the COLOR EDIT output, enter "Y" to go on to the next test. (If there is a problem with the display, enter "N" here, and the Frame A Test will repeat, allowing you to further examine the malfunction.)

Step 8: After the Frame A anti-alias level test has been completed and you've entered "N", the system will respond with Figure 4-20 "B".



```
Anti-Alias (Primary & Mix    16:57:07
Display Logic) Diagnostics

Frame A Test

16 Boxes in mix buffer of varying
intensity should be seen, but with
primary intensity = F.  Enter Y or
N.  Use color keys to change color.

Hit ESC to exit to next test.
```

Figure 4-20 "B". Anti-Alias Diagnostics Menu #3

Step 9: Observe the COLOR EDIT output and look for anomalies such as blank (missing) boxes, or incorrect levels.

Step 10: If you entered "Y" in Step 9, the system will go on to the Frame B tests, which are identical to the Frame A tests. Go back to Step 2 and follow the same procedures used for Frame A to test Frame B.

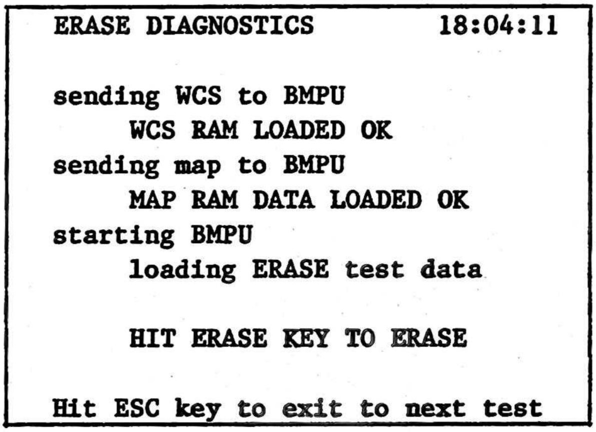
Step 11: After the Frame B tests are completed, the system will prompt with:

Do you wish to try it again? Enter Y or N

To run the entire diagnostic again, enter Y. To return to the Display & Cursor main menu, enter N.

4.3.3.4 <u>**Erase Diagnostics**</u> The erase diagnostic tests the erase function by writing all four frame buffers with F's, checking all four frame buffers, then the BMPU issues an erase command. The CPU then confirms the erase by checking the frame buffer. Also, the technician can confirm the erase by checking the program output. To run this test, follow this procedure:

Step 1: From the Frame Buffer Diagnostics main menu, select "4" to select Erase Diagnostics. The system will load the test data, then display Figure 4-21:



```
ERASE DIAGNOSTICS         18:04:11

sending WCS to BMPU
     WCS RAM LOADED OK
sending map to BMPU
     MAP RAM DATA LOADED OK
starting BMPU
     loading ERASE test data

     HIT ERASE KEY TO ERASE

Hit ESC key to exit to next test
```

Figure 4-21. Erase Diagnostics Menu #1

Step 2: Observe the COLOR EDIT output on a monitor. The screen should be white.

Step 3: Press the ERASE key. Check the COLOR EDIT output for proper ERASE operation (the screen should be black). The system will respond with:

```
ERASE completed.
Checking Frame Buffer A, B, C, D
```

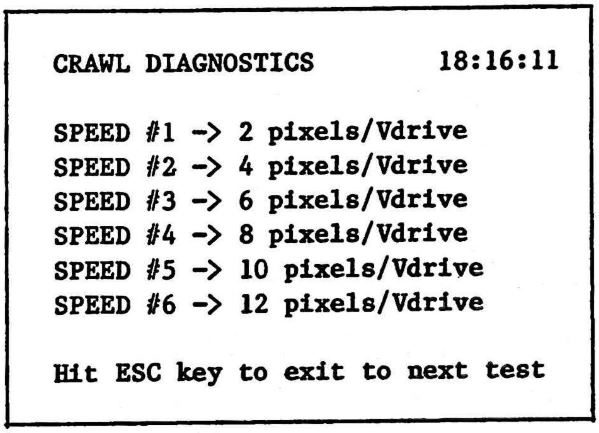
The frame buffer tests will take several moments, then the SCRIBE will indicate pass/fail. After the check, the system, will respond with:

```
Do you wish to try this test again?  ENTER Y or N
```

To run the test again, enter "Y". To return to the Frame Buffer main menu, enter "N".

4.3.3.5 **CRAWL Diagnostics** The CRAWL diagnostic tests the CRAWL hardware by issuing CRAWL commands, and observing the program output for proper operation. This test allows for variable CRAWL speeds.

Step 1: From the Frame Buffer Diagnostics main menu, select "5" to select the CRAWL Diagnostics. The system displays the speed choices available (Figure 4-22):

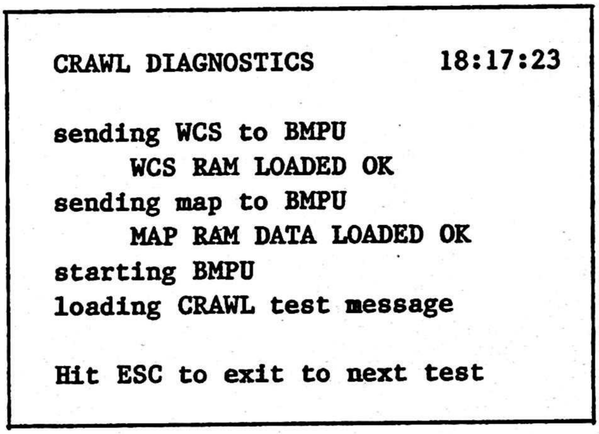


```
CRAWL DIAGNOSTICS            18:16:11

SPEED #1 -> 2 pixels/Vdrive
SPEED #2 -> 4 pixels/Vdrive
SPEED #3 -> 6 pixels/Vdrive
SPEED #4 -> 8 pixels/Vdrive
SPEED #5 -> 10 pixels/Vdrive
SPEED #6 -> 12 pixels/Vdrive

Hit ESC key to exit to next test
```

Figure 4-22. Crawl Diagnostics Menu #1

Step 2: Observe the COLOR EDIT output on a monitor.

Step 3: Select a crawl speed from the SCRIBE Address Keypad. The system will respond with Figure 4-23:



```
CRAWL DIAGNOSTICS            18:17:23

sending WCS to BMPU
     WCS RAM LOADED OK
sending map to BMPU
     MAP RAM DATA LOADED OK
starting BMPU
loading CRAWL test message

Hit ESC to exit to next test
```

Figure 4-23. Crawl Diagnostics Menu #2

After a few moments, the system will respond with:

```
HIT CRAWL TO BEGIN CRAWLING
```

Step 4: Press the CRAWL key to start the crawl message. Observe the COLOR EDIT display for any anomalies.

Notes

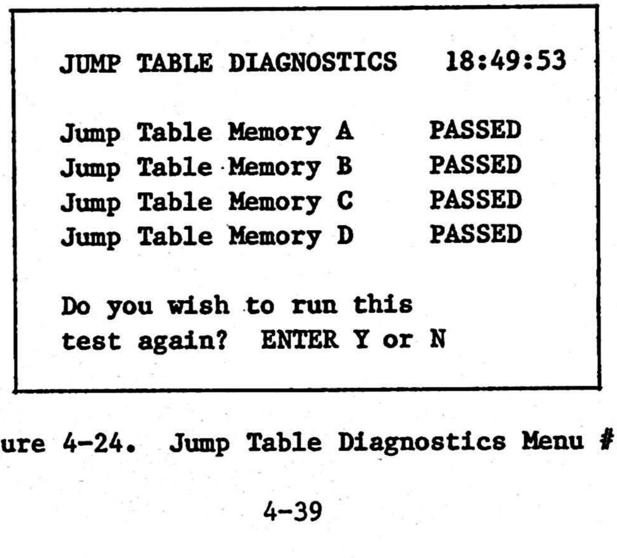
You can change the crawl speed at any time during this test by entering a new speed value on the SCRIBE Address Keypad.

If any errors occur during crawl operation, run the test repeatedly to isolate the difficulty. Once an error has been isolated, contact CHYRON Customer Service for further information.

Step 5: When you are satisfied with CRAWL operation, press the ESC key to exit to the Frame Buffer main menu.

4.3.3.6 **Jump Table Diagnostics** The jump table diagnostics perform memory tests on each of the four jump table memories. (The jump table RAM is used for operations such as ROLL and CRAWL). To run these tests, follow this procedure:

Step 1: From the Frame Buffer main menu, select "6" to enter and start the Jump Table diagnostics. The system will respond with Figure 4-24:



```
JUMP TABLE DIAGNOSTICS   18:49:53

Jump Table Memory A      PASSED
Jump Table Memory B      PASSED
Jump Table Memory C      PASSED
Jump Table Memory D      PASSED

Do you wish to run this
test again?  ENTER Y or N
```

Figure 4-24. Jump Table Diagnostics Menu #1

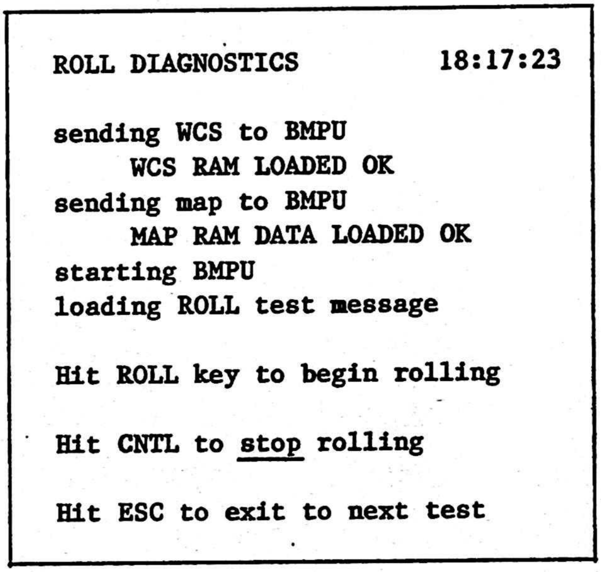
Step 2: If Jump Table Memories A, B, C, and D all passed the test, enter "N" here to return to the Frame Buffer Diagnostics main menu. If any of the four jump table memories did not pass, enter "N" here to repeat the tests.

Note

If one or more of the Jump Table memories consistently fails the test, the particular jump table memory is faulty and must be replaced. Contact CHYRON Customer Service for more information.

4.3.3.7 ROLL Diagnostics The ROLL diagnostic tests the ROLL hardware by issuing ROLL commands, and having the technician observe the program output for proper operation. This test does not use the BMPU section to perform the roll, but reads a message into the frame buffer and changes the jump table values to roll the message.

Step 1: From the Frame Buffer Diagnostics main menu, select "7" to select the ROLL Diagnostics. The system reads the roll message into the frame buffer, and responds with Figure 4-25:



```
ROLL DIAGNOSTICS            18:17:23

sending WCS to BMPU
     WCS RAM LOADED OK
sending map to BMPU
     MAP RAM DATA LOADED OK
starting BMPU
loading ROLL test message

Hit ROLL key to begin rolling

Hit CNTL to stop rolling

Hit ESC to exit to next test
```

Figure 4-25. Roll Diagnostics Menu #1

Step 2: Observe the COLOR EDIT output on a monitor.

Step 3: After the roll message is properly loaded, press the ROLL key. The system will begin the roll procedure, which can be observed on the COLOR EDIT output.

To stop the roll message, press the CNTL key.

A = Display Frame A.
B = Display Frame B.

Step 4: Examine the COLOR EDIT output for any changes. Press the "A" key to display the Frame A output. Press the "B" key to display the Frame B output.

Step 5: After roll operation has been verified, press the ESC key to return to the Frame Buffer diagnostics main menu.

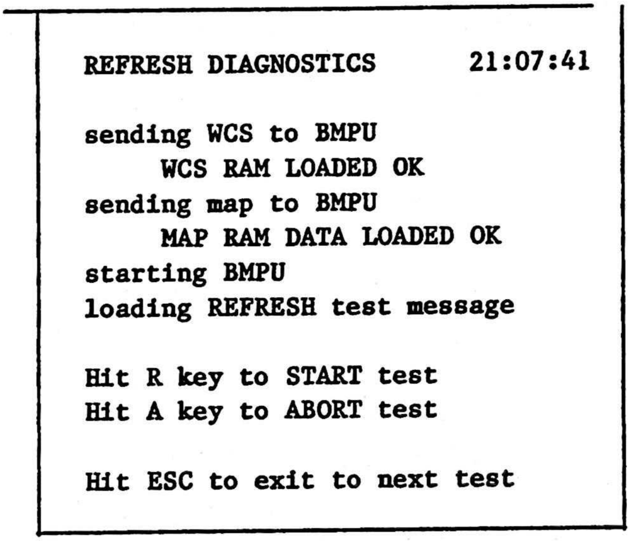
Note

Any error that occurs during roll operation will be recorded in the SCRIBE error log. The error log will note the date, time, and nature of the error. If a roll error consistently occurs during this test, the Frame Buffer roll/jump table logic is faulty. Contact CHYRON Customer Service for further instructions.

4.3.3.8 Refresh Diagnostics The Frame Buffer Refresh diagnostics operate by displaying a message on the program output. This message is then observed for any changes (fading) over a thirty-second period. Any changes or fading on the display would indicate a problem with the refresh logic.

To perform this test, follow this procedure:

Step 1: From the Frame Buffer diagnostics main menu, select "8" to enter the Refresh Diagnostics. The system will respond with Figure 4-26:



```
REFRESH DIAGNOSTICS         21:07:41

sending WCS to BMPU
     WCS RAM LOADED OK
sending map to BMPU
     MAP RAM DATA LOADED OK
starting BMPU
loading REFRESH test message

Hit R key to START test
Hit A key to ABORT test

Hit ESC to exit to next test
```

Figure 4-26. Refresh Diagnostics Menu #1

Step 2: Observe the COLOR EDIT output on a monitor.

Step 3: Press the "R" key to start the test. (To abort the test for any reason, press the "A" key.) The following prompt appears on the Prompts monitor:

Message will be observed for 30 seconds.

The count of seconds decreases as the test progresses. Observe the COLOR EDIT output for any changes to the display. At the end of the countdown, the following message appears:

Message should still be visible.

A = Display Frame A.
B = Display Frame B.

Step 4: Examine the COLOR EDIT output for any changes. Press the "A" key to display the Frame A output. Press the "B" key to display the Frame B output.

If there are no changes in either frame and no fading is evident, then the refresh logic is functioning correctly. If there are any changes on the display, the refresh logic is faulty. Contact CHYRON Customer Service for further instructions.

4.4 BITSLICE (BMPU) DIAGNOSTICS

4.4.1 GENERAL

This paragraph describes the bitslice (BMPU) diagnostics for the SCRIBE system. This paragraph includes a complete listing of all applicable subtests, operating instructions for the diagnostic programs, and instructions for how to interpret the results of each subtest.

4.4.2 DESCRIPTIONS OF SUBTESTS

Table 4-3 contains a list of subtests associated with the bitslice (BMPU) diagnostic programs, as well as a brief description for each.

Table 4-3. Bitslice (BMPU) Diagnostics Subtests

Subtest Name	Description
VME Interface Diagnostics	Tests the VME interface by write/reading data words over the interface. This diagnostic tests both the VME interface and the nine shift registers on the BMPU board.
VMX (Font Memory) Interface Diagnostics	This diagnostic tests the VMX (Font Memory) bus by write-reading data across the bus, then testing the data using the VME bus.
VMX (Frame Buffer) Interface Diagnostics	This diagnostic tests the VMX/Frame Buffer interface by write-reading from the BMPU to the Frame Buffer using the VMX bus, then testing the data for accuracy over the VME bus.

Table 4-3. Bitslice (BMPU) Diagnostics Subtests, continued

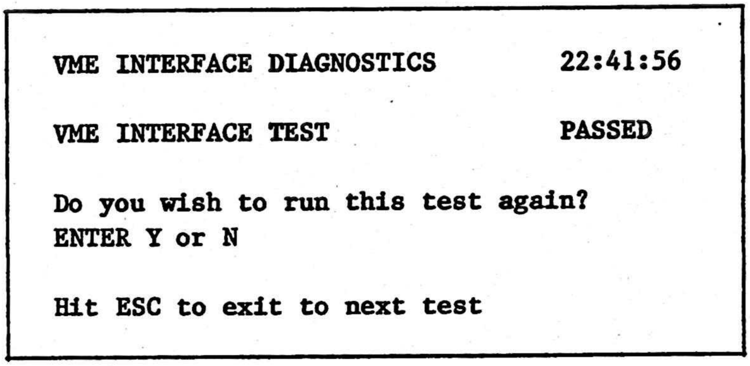
Subtest Name	Description
WCS RAM Diagnostic	This diagnostic tests the WCS RAM on the BMPU by writing data from the diagnostic disk to both the WCS (on the BMPU) and the CPU. Then, this data is read from the WCS by the CPU and compared for accuracy.
MAP RAM Diagnostic	This diagnostic tests the MAP RAM on the BMPU by writing data from the disk diagnostic disk to both the MAP RAM (on the BMPU) and the CPU. The data is read from the MAP RAM by the CPU, and compared for accuracy.
Operational Diagnostic	This diagnostic tests the BMPU for operation by giving the BMPU code to execute and a RUN instruction. Then, the diagnostic tests for the proper interrupt vector (indicating correct BMPU operation).

4.4.3 OPERATIONAL INSTRUCTIONS

This paragraph contains operational instructions for how to operate the bitslice (BMPU) diagnostics, which are listed and described in paragraph 4.4.2.

4.4.3.1 VME Interface Diagnostics The VME interface diagnostics test the BMPU - CPU VME interface by having the CPU write-read data words across the VME bus to the BMPU. To do this, the CPU first writes data word 5555 to the BMPU using the SSRLD instruction. Next, AAAA is written in the same manner. The next seven data words written are 0000. This process is necessary due to the nine shift registers on the BMPU board. Once loaded with data, the shift registers are read using the RSSR instruction. This test checks not only the VME bus, but also tests the BMPU shift registers for proper operation.

Step 1: From the Bitslice Diagnostics main menu (#3 from the SCRIBE DIAGNOSTICS menu), enter "1" to select VME Interface Diagnostics. The system will respond with Figure 4-27:



```
VME INTERFACE DIAGNOSTICS          22:41:56

VME INTERFACE TEST                 PASSED

Do you wish to run this test again?
ENTER Y or N

Hit ESC to exit to next test
```

Figure 4-27. VME Interface Diagnostics Menu #1

Step 2: If the VME interface passes the test, enter N to return the the Bitslice main menu.

If the VME interface fails this test, repeat the test to isolate the problem. Also, test the VME interface through the CPU and/or Frame Buffer diagnostics. Once the problem has been isolated, contact CHYRON Customer Service for assistance.

4.4.3.2 **VMX (Font Memory) Interface Diagnostics** In this diagnostic, the BMPU will test the VMX interface to the Font Memory by write-reading data across the VMX bus. Then, the CPU verifies the written data across the VME bus.

Step 1: From the Bitslice Diagnostics main menu (#3 from the SCRIBE DIAGNOSTICS menu), enter "2" to select VMX (Font Memory) Interface Diagnostics. The system will respond with Figure 4-28:

```
 VMX (FONT MEMORY) INTERFACE DIAGNOSTICS

   Sending WCS to BMPU
 WCS RAM DATA LOADED OK
   Sending map to BMPU
 MAP RAM DATA LOADED OK
   Starting BMPU

 WCS & MAP data loaded to BMPU correctly

 VMX INTERFACE (FONT MEMORY)     PASSED

Font memory test data verified using VME bus

Do you wish to run this test again?
ENTER Y or N
```

Figure 4-28. VMX Interface Diagnostic Menu #1

Step 2: If the VMX (font memory) interface passes the test, enter N here to return the the Bitslice main menu.

If this interface <u>fails</u> the test, repeat the test to isolate the difficulty. Also, test the VMX interface through the Font Memory diagnostic subgroup. Once the difficulty has been isolated, contact CHYRON Customer Service for further information.

4.4.3.3 VMX (Frame Buffer) Interface Diagnostics In this diagnostic, the BMPU will test the VMX interface to the Frame Buffer by write-reading data across the VMX bus. Then, the CPU verifies the written data across the VME bus.

Step 1: From the Bitslice Diagnostics main menu (#3 from the SCRIBE DIAGNOSTICS menu), enter "3" to select VMX (Frame Buffer) Interface Diagnostics. The system will respond with Figure 4-29:

```
 VMX (Frame Buffer) INTERFACE DIAGNOSTICS

   Sending WCS to BMPU
 WCS RAM DATA LOADED OK
   Sending map to BMPU
 MAP RAM DATA LOADED OK
   Starting BMPU

 WCS & MAP data loaded to BMPU correctly

 VMX INTERFACE (Frame Buffer)     PASSED

Frame Buffer test data verified using VME bus

Do you wish to run this test again?
ENTER Y or N
```

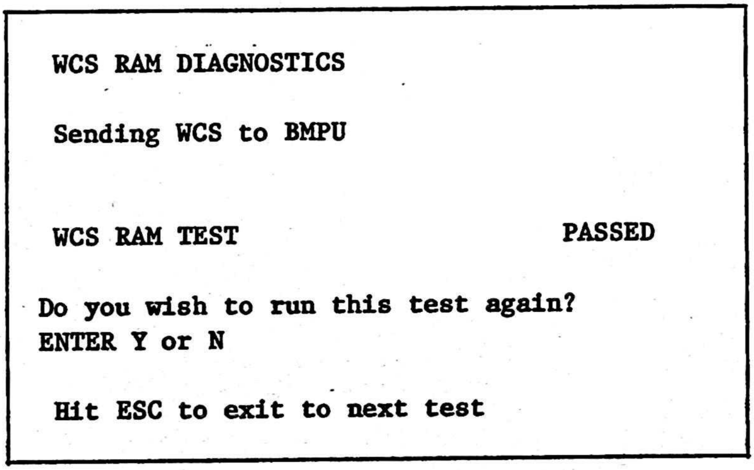
Figure 4-29. VMX Interface Diagnostics Menu #2

Step 2: If the VMX (Frame Buffer) interface passes the test, enter N here to return the the Bitslice main menu.

If this interface fails the test, repeat the test to isolate the difficulty. Also, test the VMX interface through the Frame Buffer diagnostic subgroup. Once the difficulty has been isolated, contact CHYRON Customer Service for further information.

4.4.3.4 <u>WCS RAM Diagnostics</u> In this diagnostic, the BMPU will test the WCS RAM by using code written from the diagnostic disk. The code is written to both the WCS and the CPU. Then, the CPU reads the code from the WCS, and performs a comparison to confirm proper WCS operation.

Step 1: From the Bitslice Diagnostics main menu (#3 from the SCRIBE DIAGNOSTICS menu), enter "4" to select WCS RAM Diagnostics. The system will respond with Figure 4-30:



```
 WCS RAM DIAGNOSTICS

 Sending WCS to BMPU


 WCS RAM TEST                      PASSED

Do you wish to run this test again?
ENTER Y or N

 Hit ESC to exit to next test
```

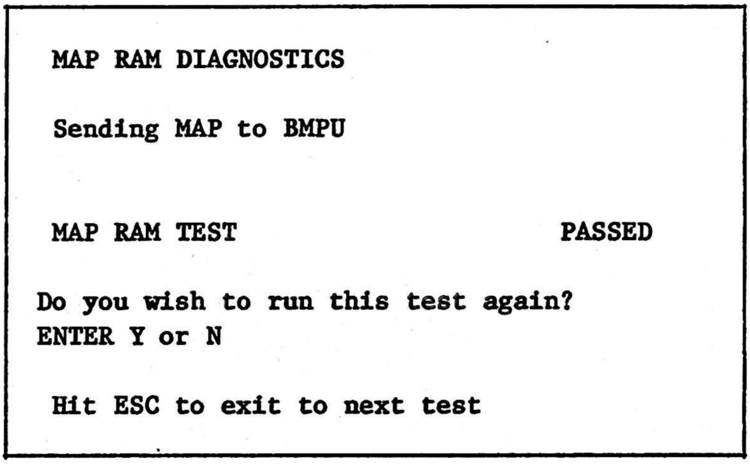
Figure 4-30. WCS RAM Diagnostics Menu #1

Step 2: If the WCS RAM passes the test, enter N here to return the the Bitslice main menu.

If the WCS RAM <u>fails</u> the test, repeat the test to isolate the difficulty. Once the difficulty has been isolated, contact CHYRON Customer Service for further information.

4.4.3.5 Map RAM Diagnostics In this diagnostic, the BMPU will test the MAP RAM by using code written from the diagnostic disk. The code is written to both the MAP RAM and the CPU. Then, the CPU reads the code from the MAP RAM, and performs a comparison to confirm proper MAP RAM operation.

Step 1: From the Bitslice Diagnostics main menu (#3 from the SCRIBE DIAGNOSTICS menu), enter "5" to select MAP RAM Diagnostics. The system will respond with Figure 4-31:



```
  MAP RAM DIAGNOSTICS

  Sending MAP to BMPU


  MAP RAM TEST                        PASSED

 Do you wish to run this test again?
 ENTER Y or N

  Hit ESC to exit to next test
```

Figure 4-31. MAP RAM Diagnostic Menu #1

Step 2: If the MAP RAM passes the test, enter N here to return the the Bitslice main menu.

If the MAP RAM fails the test, repeat the test to isolate the difficulty. Once the difficulty has been isolated, contact CHYRON Customer Service for further information.

4.4.3.6 **Operational Diagnostics** In this diagnostic, the BMPU is tested in the following manner: The BMPU is provided with code to execute, and is given the RUN instruction. If the BMPU is functioning properly, an interrupt vector of $81 will be executed. If the BMPU is not functioning properly, then a fail interrupt vector of $82 will be executed. If, however, the BMPU fails to interrupt before a timeout variable, then the BMPU is also considered to be non-functional and fails the operational test.

Step 1: From the Bitslice Diagnostics main menu (#3 from the SCRIBE DIAGNOSTICS menu), enter "6" to select Operational Diagnostics. The system will respond with Figure 4-32:

```
              OPERATIONAL DIAGNOSTICS

   Sending WCS to BMPU
 WCS RAM DATA LOADED OK
   Sending MAP to BMPU
 MAP RAM DATA LOADED OK
   Starting BMPU

 WCS & MAP data loaded to BMPU correctly

 BMPU OPERATIONAL TEST           PASSED

Do you wish to run this test again?
ENTER Y or N
```

Figure 4-32. Operational Diagnostics Menu

Step 2: If the BMPU passes the test, enter N here to return the the Bitslice main menu.

If the BMPU fails the test, repeat the test to isolate the difficulty. Once the difficulty has been isolated, contact CHYRON Customer Service for further information.

4.5 FONT MEMORY DIAGNOSTICS

4.5.1 GENERAL

This paragraph describes the font memory diagnostics for the SCRIBE system. This paragraph includes a complete listing of all applicable subtests, operating instructions for the diagnostic programs, and instructions for how to interpret the results of each subtest.

4.4.2 DESCRIPTIONS OF SUBTESTS

Table 4-4 contains a list of subtests associated with the font memory diagnostic programs, as well as a brief description for each.

Table 4-4. Font Memory Diagnostics Subtests

Subtest Name	Description
VME Interface Diagnostics	Tests the VME interface by write/reading data words over the interface. This interface is tested when the memory is tested and also when parity interrupt logic is tested.
VMX (Font Memory) Interface Diagnostics	This diagnostic tests the VMX (Font Memory) bus with a memory/address decode test performed by the BMPU. The BMPU write/reads the font memory over the VMX bus, and the CPU checks the write over the VME bus.

Table 4-4. Font Memory Diagnostics Subtests, continued

Subtest Name	Description
Parity Interrupt Logic Diagnostics	This diagnostic tests the Font Memory parity interrupts by setting an interrupt level, forcing a parity error, and checking that the proper parity interrupt was received. Upon receiving the proper interrupt, the next priority level interrupt is enabled and the test is repeated. The test is repeated for all five interrupt levels.
Memory Diagnostics	This test is the standard memory test. First, the entire font memory is write/read with one's, then the entire memory is write/read with zero's. This test also tests the VME and VMX busses, as well as BMPU and CPU operation.
Address Decode Diagnostics	This test functions by write-reading addresses in the font memory, and indicating proper address decode operation.

Table 4-4. Font Memory Diagnostics Subtests, continued

Subtest Name	Description
Refresh Diagnostics	The refresh diagnostics test the font memory's refresh logic by write/reading data, waiting 30 seconds, then reading the memory again. A refresh logic malfunction is indicated if the second read is in error.
BMPU/VME Simultaneous Access	In this test, the BMPU is instructed to write/read the font memory while the CPU is instructed to do the same across the VME bus at different memory locations.

4.5.3 OPERATIONAL INSTRUCTIONS

This paragraph contains operational instructions for how to operate the font memory diagnostics, which are listed and described in paragraph 4.5.2.

4.5.3.1 VME Interface Diagnostics The VME interface diagnostics test the Font Memory - CPU VME interface by having the CPU write-read data words across the VME bus to the font memory. If the CPU detects an error in its read, then the VME interface is posted as failing. If a VME interface failure occurs during this test, be sure to perform the Font Memory memory diagnostics before proceeding.

Step 1: From the Font Memory Diagnostics main menu, enter "1" to select the VME Interface Diagnostics. The system will respond with Figure 4-33:

```
VME INTERFACE DIAGNOSTICS          22:41:56

Note:  PARITY is ENABLED

VME / FONT MEMORY INTERFACE        PASSED

Do you wish to run this test again?
ENTER Y or N
```

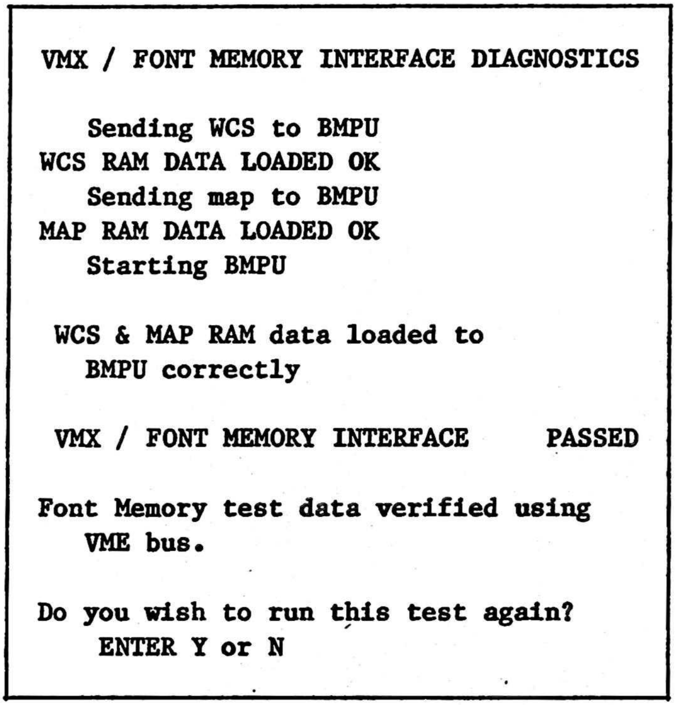
Figure 4-33: FONT MEMORY DIAGNOSTICS: VME Interface Menu

Step 2: If the VME interface passes the test, enter N to return to the Font Memory Diagnostics main menu.

If the VME interface <u>fails</u> this test, repeat the test to isolate the difficulty. Perform the Font Memory memory diagnostics (#4 from the Font Memory main menu) to test the memory locations. Also, test the VME interface from the CPU and/or Frame Buffer diagnostic subgroups. Once the difficulty has been isolated, contact CHYRON Customer Service for more information.

4.5.3.2 **VMX Interface Diagnostics** The VMX interface diagnostics test BMPU / Font Memory communication over the VMX bus. The BMPU writes address values at a series of addresses over the VMX bus, and the CPU reads the series of addresses for the correct values over the VME bus. Thus, the VMX bus, the VME bus, the BMPU, the CPU, and the address decode logic are all tested through these diagnostics. To run these diagnostics, follow the procedure on the next page.

Step 1: From the Font Memory Diagnostics main menu, enter "2" to select the VMX Interface Diagnostics. The system will respond with Figure 4-34:



```
VMX / FONT MEMORY INTERFACE DIAGNOSTICS

   Sending WCS to BMPU
WCS RAM DATA LOADED OK
   Sending map to BMPU
MAP RAM DATA LOADED OK
   Starting BMPU

 WCS & MAP RAM data loaded to
   BMPU correctly

 VMX / FONT MEMORY INTERFACE     PASSED

Font Memory test data verified using
   VME bus.

Do you wish to run this test again?
    ENTER Y or N
```

Figure 4-34. Font Memory Diagnostics: VMX Interface Menu

Step 2: If the VMX / Font Memory interface passes the test, enter N to return to the Font Memory Diagnostics main menu.

If the VMX Font Memory interface fails this test, repeat the test to isolate the difficulty. Perform the Font Memory memory diagnostics (#4 from the Font Memory main menu) to test the memory locations. Also, test the VMX interface from the CPU and/or Frame Buffer diagnostic subgroups. Once the difficulty has been isolated, contact CHYRON Customer Service for more information.

4.5.3.3 Parity Interrupt Logic Diagnostics This diagnostic tests the Font Memory parity interrupts by setting an interrupt level, forcing a parity error, and checking that the proper parity interrupt was received. Upon receiving the proper interrupt, the next priority level interrupt is enabled and the test is repeated. The test is repeated for all five interrupt levels. To run this diagnostic, follow this procedure:

Step 1: From the Font Memory Diagnostic main menu, select "3" to enter the Parity Interrupt Logic diagnostics. The system will respond with Figure 4-35:

```
   PARITY INTERRUPT LOGIC DIAGNOSTICS

  Note:  PARITY is ENABLED

PARITY INTERRUPT LOGIC LEVEL #1   PASSED
PARITY INTERRUPT LOGIC LEVEL #2   PASSED
PARITY INTERRUPT LOGIC LEVEL #3   PASSED
PARITY INTERRUPT LOGIC LEVEL #4   PASSED
PARITY INTERRUPT LOGIC LEVEL #5   PASSED

Do you wish to run this test again?
ENTER Y or N
```

Figure 4-35. Font Memory Diagnostics: Parity Interrupt Menu

Step 2: If all five parity interrupt levels pass this test, enter N to return to the Font Memory Diagnostics main menu.

If any of the parity interrupt levels fail this test, repeat the test to isolate the difficulty. Perform the Font Memory memory diagnostics (#4 from the Font Memory main menu) to test the memory logic. Once the difficulty has been isolated, contact CHYRON Customer Service for more information.

4.5.3.4 **Memory Diagnostics** This diagnostic tests the entire Font Memory by having both the CPU and the BMPU write/read the memory with one's, then with zero's. The diagnostic is set up to allow memory testing one (512k) block at a time, or all blocks of the memory together. (NOTE: If the SCRIBE diagnostic is instructed to test a block of memory that is not present, then an error will be posted on the Prompts monitor, indicating that there is no memory present at that location.) If the diagnostic program suspects a chip, the chip will show up in the Error Log as being "SUSPECT". (Refer to paragraph 4.1.5 for more information about failures and error logging.) If such a failure occurs while operating the Memory Diagnostics, run the test again to isolate the difficulty.

CAUTION

> Any failure that specifies a chip as being "SUSPECT" should be treated with caution. Many factors can cause an otherwise good chip to appear faulty, so the pattern of failures provides a clue to the actual failure. When such a failure occurrs, contact CHYRON Customer Service or your Field Representative immediately. Do NOT attempt to replace a chip without assistance from CHYRON Customer Service as this will void the system warranty!

Step 1: From the Font Memory Diagnostic main menu, select "4" to enter the Parity Interrupt Logic diagnostics. The system will respond with Figure 4-36:

```
             MEMORY DIAGNOSTICS

  Note:  PARITY is ENABLED

 Select:
   [1]  1st 512k Block of Font Memory
   [2]  2nd 512k Block of Font Memory
   [3]  3rd 512k Block of Font Memory
   [4]  4th 512k Block of Font Memory
   [5]  All of Font Memory
```

Figure 4-36. Font Memory/Memory Diagnostics Menu

Step 2: Select the block of memory to be tested by entering the appropriate number. If you select [5] here, go on to Step 3. (In this example, assume that only the first 512k block is present in the SCRIBE.) The system will respond with:

```
Font Memory / Memory Test  1    512k Block        PASSED
```

Note

If you attempt to test a non-existent block of memory, the system will respond with:

```
No font memory found
```

Step 3: If you select "5" from the first menu, the system will test all blocks of font memory, starting with the first 512k block. If there are fewer than four 512k blocks of memory present, the system will test blocks of memory until it tries to test a non-existent block of memory. The system will post the "No Font Memory Found" error, then it will prompt with:

```
Do you wish to run this test again? ENTER Y or N
```

Step 4: If all areas of memory pass the test(s), enter "N" here to return to the Font Memory diagnostic main menu.

If any memory block fails the test, repeat the test to isolate the difficulty. Also, run the Parity Interrupt Logic test (#3 from the Font Memory diagnostic main menu) to check for any parity errors. Once the difficulty has been isolated, contact CHYRON Customer Service for more information.

4.5.3.5 **Address Decode Diagnostics** These diagnostics test the address-decode logic of the Font Memory by having both the CPU and the BMPU write/read addresses on the Font Memory board. The BMPU writes a series of address values to those addresses, then the CPU reads those addresses and looks for the proper address values. If the CPU discovers an address out of sequence, an error flag is posted, and the particular block under test fails.

Step 1: From the Font Memory Diagnostic main menu, select "5" to enter the Address Decode diagnostics. The system will respond with Figure 4-37:

```
     ADDRESS DECODE DIAGNOSTICS

  Note:  PARITY is ENABLED

 Select:
   [1]  1st 512k Block of Font Memory
   [2]  2nd 512k Block of Font Memory
   [3]  3rd 512k Block of Font Memory
   [4]  4th 512k Block of Font Memory
   [5]  All of Font Memory
```

Figure 4-37. Address Decode Diagnostic Menu

Step 2: Select the block of memory to be tested by entering the appropriate number. If you select [5] here, go on to Step 3. (In this example, assume that only the first 512k block is present in the SCRIBE.) The system will respond with:

```
Font Memory / Address Decode Test  1   512k Block   PASSED
```

Step 3: If you select "5" from the first menu, the system will test all blocks of font memory, starting with the first 512k block. The test will go through all available addresses, regrardless of whether or not the actual memory is in place. When the system has tested all available addresses, is will prompt with:

Do you wish to run this test again? ENTER Y or N

Step 4: If all areas of memory pass the test(s), enter "N" here to return to the Font Memory diagnostic main menu.

If any memory block fails the test, repeat the test to isolate the difficulty. Also, run the Memory Diagnostic test (#4 from the Font Memory diagnostic main menu) to check for any errors. Once the difficulty has been isolated, contact CHYRON Customer Service for more information.

4.5.3.6 **Refresh Diagnostics** These diagnostics test the refresh logic of the Font Memory by write/reading the Font memory, waiting 30 seconds, then checking the memory write for errors. If the CPU discovers an error, an error flag is posted, and the particular block under test fails.

Step 1: From the Font Memory Diagnostic main menu, select "6" to enter the Refresh diagnostics. The system will respond with Figure 4-38:

```
                REFRESH DIAGNOSTICS

   Note:  PARITY is ENABLED

  Select:
     [1]  1st 512k Block of Font Memory
     [2]  2nd 512k Block of Font Memory
     [3]  3rd 512k Block of Font Memory
     [4]  4th 512k Block of Font Memory
     [5]  All of Font Memory
```

Figure 4-38. Font Memory: Refresh Diagnostics

Step 2: Select the block of memory to be tested by entering the appropriate number. (In this example, assume that all blocks of memory are present in the SCRIBE.) The system will respond with:

```
Font Memory / Refresh Test  1   512k Block   PASSED
Font Memory / Refresh Test  2   512k Block   PASSED
Font Memory / Refresh Test  3   512k Block   PASSED
Font Memory / Refresh Test  4   512k Block   PASSED

Please Wait 30 Seconds
```

The system will count down thirty seconds, then the blocks will be tested again. (Note: Press ESC to exit from test before count is completed.) If all blocks pass on the second test, then the refresh logic is functioning properly. The system will respond with:

```
Do you wish to run this test again?  ENTER Y or N
```

Step 3: If all blocks of font memory passed the refresh logic test, enter N here to return to the Font Memory main menu.

If any block(s) of memory fail the test, repeat the test to isolate the difficulty. Be sure to perform the standard Memory Test (#4 from the Font Memory main menu) to ensure normal memory operation. Once the difficulty has been isolated, contact CHYRON Customer Service for further information.

4.5.3.7 **BMPU/VME Simultaneous Access Diagnostics** These diagnostics test the Font Memory's ability to be written to and read from over the VMX and VME busses, at the same time. In this test, the BMPU write-reads the font memory over the VMX bus, and the CPU write-reads the font memory over the VME bus. This tests the arbitration logic between the VME and VMX busses.

Step 1: From the Font Memory Diagnostic main menu, select "7" to start the BMPU/VME Simultaneous Access diagnostics. The system will respond with Figure 4-39:

```
     BMPU/VME SIMULTANEOUS ACCESS DIAGNOSTICS

     Note: PARITY is ENABLED
         (parity flashes for 1 second)

       Sending WCS to BMPU
     WCS RAM DATA LOADED OK
       Sending map to BMPU
      AP RAM DATA LOADED OK
       Starting BMPU

  BMPU / VME SIMULTANEOUS ACCESS TEST    PASSED

  Do you wish to run this test again?
  ENTER Y or N
```

Figure 4-39. BMPU/VME Simultaneous Access Test Menu

Step 2: If the font memory passes the BMPU/VME Simultaneous Access Test, enter N here to return to the Font Memory main menu.

If the font memory <u>fails</u> the test, repeat the test to isolate the difficulty. Be sure to perform the standard Memory Test (#4 from the Font Memory main menu) to ensure normal memory operation. Once the difficulty has been isolated, contact CHYRON Customer Service for further information.

4.6 CPU DIAGNOSTICS

4.6.1 GENERAL

This paragraph describes the CPU diagnostics for the SCRIBE system. This paragraph includes a complete listing of all applicable subtests, operating instructions for the diagnostic programs, and instructions for how to interpret the results of each subtest.

4.6.2 DESCRIPTIONS OF SUBTESTS

Table 4-5 contains a list of subtests associated with the CPU diagnostic programs, as well as a brief description for each.

Table 4-5. CPU Diagnostics Subtests

Subtest Name	Description
68010 MPU Test	Tests registers, Arithmetic Logic unit, instructions and Exception Processing using the 68010 MPU.
ROM Test	This diagnostic tests ROM by calculating a 16-bit checksum by taking the Exclusive OR of all ROM data.
RAM Test (parity disabled)	All CPU RAM above address $FFF is tested using the walking bit and pattern tests.

Table 4-5. CPU Diagnostics Subtests, continued

Subtest Name	Description
Parity Logic Test	Testing of the parity logic is performed by a variety of tests, including: incorrect parity verification, bus error generation, and Parity Error Bit (in CPU control Register) operation.
Parity RAM Test	With parity enabled, data is written to all RAM addresses and verified.
RAM Test (parity enabled)	All CPU RAM above address $FFF is tested using the walking bit and pattern tests.
CMOS RAM Test	CMOS memory is sized on 2, 4, and 8k boundaries for recundancy. When the size has been determined, it is displayed after the test message. A non-destructive memory test is then performed on the size found. The memory test consists of reading byte data, writing the complement of that data, verifying the data, restoring the original data, and verifying that data.

Table 4-5. CPU Diagnostics Subtests, continued

Subtest Name	Description
Serial Port Test	Since one of the several serial ports is used as the system console, this test runs the internal loopback test on the two VME117 ports. The messages "This is a test of Port #1" and This is a test of Port #2" are sent to the appropriate ports and verified. Due to the characteristics of the loopback mode, these characters are also sent to any device connected to the VME117 serial ports.
PTM Test	In this test, timers 1, 2, and 3 are set for maximum count and are allowed to time out with outputs disabled. Timers 1, 2, and 3 (if operating properly) generate interrupts when they time out.
Real Time Clock Test	This test checks the MM58274 chip for roll-over in time from: 99:12:31:23:59:59 Day 7 to 00:01:01:00:00:00 Day 1

Table 4-5. CPU Diagnostics Subtests

Subtest name	Description
68881 (co-processor) Test	The optional 68881 co-processor is tested for; if present, several data conversion tests and a multiplication test are performed.
SCSI Test	A verification of the SCSI chip is performed; then its registers are read, reset, and read again.
Abort Button Test	The ABORT button on the MVME117 front panel is tested. The operator uses the button to generate an abort; if an abort is detected, then the ABORT switch passes.
LED Test	This test checks control register fail bit for correct operation. The operator visually verified Fail LED operation.

4.6.3 OPERATIONAL INSTRUCTIONS

This paragraph contains operational instructions for how to operate the CPU diagnostics, which are listed and described in paragraph 4.6.2. The series of tests that comprise the CPU Diagnostics are executed immediately upon entering the diagnostics. Any failures with the CPU and associated hardware are flagged in the Error Log, after which the CPU diagnostics continue.

Note

The SCRIBE Diagnostics Disk must be re-booted (re-loaded into the system) after the CPU Diagnostics are run. A message to this effect is displayed before the tests are started.

To start the CPU Diagnostics, follow this procedure:

Step 1: From the SCRIBE Diagnostics main menu, select "5" to enter the CPU Diagnostics. The system will respond with Figure 4-40:

```
                CPU DIAGNOSTICS


CAUTION!! This is a DESTRUCTIVE test
Real-Time Clock Data will be LOST
Diagnostics must be REBOOTED following
this test.

Do you wish to continue? Enter Y or N
```

Figure 4-40. CPU Diagnostics Menu #1

Step 2: If you do not wish to continue this test, enter "N" here, to return to the SCRIBE Diagnostics main menu.

To proceed with the CPU diagnostics, enter "Y" here. The system will respond with Figure 4-41:

```
              CPU DIAGNOSTICS

68010 MPU Test                      PASSED
ROM Test                            PASSED
RAM Test - parity disabled -        PASSED
Parity Logic Test                   PASSED
Parity RAM Test                     PASSED
RAM Test - parity enabled -         PASSED
CMOS Memory Test (Size: 8k)         PASSED
Serial Port Test                    PASSED
PTM Test                            PASSED
```

Figure 4-41. CPU Diagnostics Menu #2

This display will appear for a few seconds, then the following display (Figure 4-42, containing the remaining tests) appears:

```
                CPU DIAGNOSTICS

     Real Time Clock Test               PASSED
     68881 Test                       BYPASSED
     SCSI Test                          PASSED
     Abort Button Test

     Press VME117 Abort Button
```

Figure 4-42. CPU Diagnostics Menu #3

Note

If the CPU Abort button is not accessible, press a <CR> to bypass this test.

Step 3: Locate the ABORT button on the MVME117 board front panel. Press this button. If the button functions properly and generates an abort signal, the system will respond with:

```
Abort Button Test          PASSED
```

If the button fails, or is not pressed (or the test is not bypassed with a <CR> keystroke), the system will respond with:

```
No abort signal was received.
```

If no abort is received, the test is listed as FAILED, and the remainder of the CPU Diagnostics are carried out. The system will respond with Figure 4-43:

```
                  CPU DIAGNOSTICS

     Real Time Clock Test              PASSED
     68881 Test                      BYPASSED
     SCSI Test                         PASSED
     Abort Button Test                 PASSED
     LED Test:

  Is FAIL light off? Enter Y or N or <CR>
```

Figure 4-43. CPU Diagnostics Menu #4

Note

If the VME117 FAIL light is not accessible, press a <CR> to bypass this test.

Step 3: Locate the FAIL light on the MVME117 board front panel. If the light is on, enter "N" here, and the system will log the error. If the FAIL light is off, enter "Y" here. The system will respond with:

```
Is FAIL light on?  Enter Y or N or <CR>
```

Step 4: If the FAIL light is off, enter "N" here, and the system will log the error. If the FAIL light is on, enter "Y" here and the system will respond with:

```
    LED Test                 PASSED

CPU Test is completed, Diagnostic Disk must be rebooted
```

Note

If any error(s) occurs while running the CPU Diagnostics, repeat the test to isolate the difficulty. Contact CHYRON Customer Service for more information on repair/replacement.

4.7 SCRIBE KEYBOARD DIAGNOSTICS

4.7.1 GENERAL

This paragraph describes the keyboard diagnostics for the SCRIBE system. This paragraph includes a complete listing of all applicable subtests, operating instructions for the diagnostic programs, and instructions for how to interpret the results of each subtest.

4.7.2 DESCRIPTIONS OF SUBTESTS

Table 4-6 contains a list of subtests associated with the SCRIBE keyboard diagnostic programs, as well as a brief description for each.

Table 4-6. SCRIBE Keyboard Diagnostic Subtests

Subtest Name	Description
ASCII Code / Function Description Test	This test allows the operator to check individual keys for proper operation. When a key on the keyboard is pressed, the SCRIBE echos the ASCII code for the key, and the function description.
Keyboard Interrupt Test	This test allows the operator to check that the proper interrupts are generated when keys on the

4.7.3 OPERATIONAL INSTRUCTIONS

This paragraph contains operational instructions for how to operate the SCRIBE Keyboard Diagnostics, which are listed and described in paragraph 4.7.2.

4.7.3.1 <u>ASCII Code/Function Description Test</u> This test allows the operator to verify individual keys for proper operation. When a key is pressed, the Prompts Monitor displays the ASCII code for the key, as well as the key's function description. If a key does not operate, or sends an incorrect code, contact CHYRON Customer Service for assistance.

To run this test, follow this procedure:

Step 1: From the SCRIBE Diagnostics main menu, enter "6" to select Keyboard Diagnostics. The system will respond with Figure 4-44:

```
         SCRIBE KEYBOARD DIAGNOSTICS

   Select KEY, check ASCII CODE,
   check FUNCTION DESCRIPTION

   Select RCD to exit to KEYBOARD
   INTERRUPT TEST

   Hit ESC to exit to next test
```

Figure 4-44. Keyboard Diagnostics Menu #1

Step 2: Test the keyboard by pressing keys one at a time. Each time a key is pressed, the system will respond with the ASCII code and the function description. (Here, the Spacebar was pressed. The system responded with:)

```
$20    ->  SPACE BAR
```

Continue testing until all keys have been tested, then press the RCD key to go on to the next test.

Note

If any key does not operate correctly, test it repeatedly, check the contacts, and try to restore function. If the key still does not operate, contact CHYRON Customer Service for information about repair/replacement.

4.7.3.2 Keyboard Interrupt Test This test allows the operator to check that individual keys generate the proper interrupt signals for the CPU. When a key is pressed, the Prompts Monitor displays the interrupts generated.

Do not attempt to press more than three keys at once, or else the SCRIBE diagnostics will abort. A message to this effect is generated on the Prompts monitor.

To run the test, follow this procedure:

Step 1: From the Keyboard Diagnostics, press the RCD key to select the Keyboard Interrupt Test. The system will respond with Figure 4-45:

```
      SCRIBE KEYBOARD DIAGNOSTICS

   Hit key to test i/o interrupts.
   Do NOT hit more than three keys.

   Hit ESC to exit to next test
```

Figure 4-45: Keyboard Diagnostics Menu #2

Step 2: Test the keyboard interrupts generated by pressing keys one at a time. Each time a key is pressed, the system will list the interrupts generated by the keystroke. After each key is pressed, the system responds with:

```
Channel  B  Tx  Buffer           EMPTY           Interrupt
Channel  B  Rx  buffer  CHARACTER AVAILABLE      Interrupt
```

Continue testing until all keys have been tested. Each key should provide the same interrupts. When finished, press the ESC key to return to the SCRIBE Diagnostics main menu.

Note

If any key does not operate correctly, test it repeatedly, check the contacts, and try to restore function. If the key still does not operate, contact CHYRON Customer Service for information about repair/replacement.

4.8 TRANSITION BOARD DIAGNOSTICS

4.8.1 GENERAL

This paragraph describes the transition board diagnostics for the SCRIBE system. This diagnostic requires that two switches be hooked up to the General-Purpose Interface (GPI) connector on the SCRIBE backplane. If these switches are not already hooked up, you must construct a set of test switches in order to proceed. Refer to the SCRIBE Operator Manual, Part I (Section II), for instructions on how to wire the test swiches.

4.8.2 DESCRIPTIONS OF SUBTESTS

Table 4-7 contains a list of subtests associated with the transition board diagnostic programs, as well as a brief description for each.

Table 4-7. Transition Board Diagnostics Subtests

Subtest Name	Description
DCD Interrupt (S1) Test	This test checks the Transition Board for a DCD interrupt when GPI switch S1 is closed.
CTS Interrupt (S2) Test	This test checks the Transition Board for a CTS interrupt when GPI switch S2 is closed.

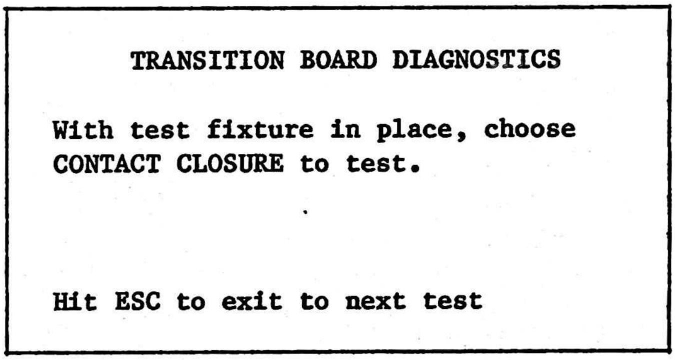
4.8.3 OPERATIONAL INSTRUCTIONS

This paragraph contains instructions for how to operate the transition board diagnostics, which are listed and described in paragraph 4.8.2.

4.8.3.1 GPI Interrupt Test The GPI interrupt test allows the operator to see if the two GPI interrupt switches (S1, S2) generate the proper interrupts when closed. (Be careful to press only one switch at a time! If both switches are closed at once, the diagnostics disk must be re-booted.)

To run this test, follow this procedure:

Step 1: From the SCRIBE Diagnostics main menu, enter "7" to select Transition Board diagnostics. The system will respond with Figure 4-46:



```
        TRANSITION BOARD DIAGNOSTICS

   With test fixture in place, choose
   CONTACT CLOSURE to test.



   Hit ESC to exit to next test
```

Figure 4-46. Transition Board Diagnostics Menu

Step 2: Be sure that the test fixture is hooked up. Press switch S1. The system will respond with:

```
DCD Interrupt has occurred,  SW1 was closed.
```

If the proper interrupt did not occur, check the test fixture wiring and check that the GPI connector is seated properly on the SCRIBE backplane. If all wiring checks out as operational contact CHYRON Customer Service for more information.

Step 3: Press GPI switch S2. The system will respond with:

CTS Interrupt has occurred. SW2 was closed.

If the proper interrupt did not occur, check the test fixture wiring and check that the GPI connector is seated properly on the SCRIBE backplane. If all wiring checks out as operational contact CHYRON Customer Service for more information.

If the proper interrupt did occur, go on to the next subtest.

4.9 DISASSEMBLY INSTRUCTIONS

4.9.1 GENERAL

This paragraph describes how to remove and replace boards and subassemblies of the SCRIBE system.

CAUTION!!!

Boards and subassemblies of the SCRIBE system may be damaged by improper handling. Exercise all precautions against board or subassembly damage including static discharge damage. Be careful not to use excessive force in removal or replacement of equipment, and guard against personal injury from electrical shock. As a general rule, never work on powered-up equipment, and if you must, always work with another person who is capable of administering aid in case of electrical shock injury.

The SCRIBE system contains two types of circuit boards. The large boards (Display & Cursor, Frame Buffers, Sync Gen, BMPU) are referred to as "9U" boards, and the smaller boards (CPU, Dual Ported Memory, Transition Board) are referred to as "6U" boards. [The "U" designation is a standard card-cage board size designation.]

In addition to the circuit boards, the SCRIBE system contains the Disk Systems Subassembly, which contains the internal floppy disk drive(s), the Winchester hard disk drive, and the primary disk controller. Also, the video encoder board for the system is located on the back door of the SCRIBE mainframe.

4.9.2 BEFORE DISASSEMBLY

Before proceeding with any removal/[illegible]ion procedure, check that the following conditions exist:

- System is off and A/C power is disconnected
- Work area is well lighted
- Work area is dust and static free

Note

If you are removing a faulty board or subassembly with the intent to ship it back to CHYRON for repair, make sure you have obtained a Material Return Authorization by calling or writing the factory. If you ship equipment without this authorization, it will be returned to you, unopened, at your cost. Therefore, avoid delay by obtaining authorization before shipment. To obtain a Material Return Authorization (MRA), refer to paragraph 4.10.

4.9.3 REMOVAL/INSTALLATION OF 6U CIRCUIT BOARDS

The 6U circuit boards of the SCRIBE system are the MVME117 CPU Board, Transition Board, Dual Ported Memory (Font Memory) Board, and CPU Transition Board (located in the rear of the mainframe). These 6U boards all share the same type of mounting hardware.

To remove any of these boards, follow this procedure.

Step 1: Refer to Figure 4-47. Locate the small slot-head screws at the top and bottom of the board's mounting panel.

Step 2: Loosen the slot-head screws that secure the board. These screws are the half-thread variety, so they will not come loose from the board itself.

Step 3: Grasp the extractor handles at the top and bottom of the board's mounting panel. Gently pull both handles straight out from the chassis. Wiggle the handles if necessary to release the board.

Step 4: Carefully remove the board from the mainframe. Be especially careful not to damage the board edges and corners during handling.

To install a 6U board, reverse this procedure.

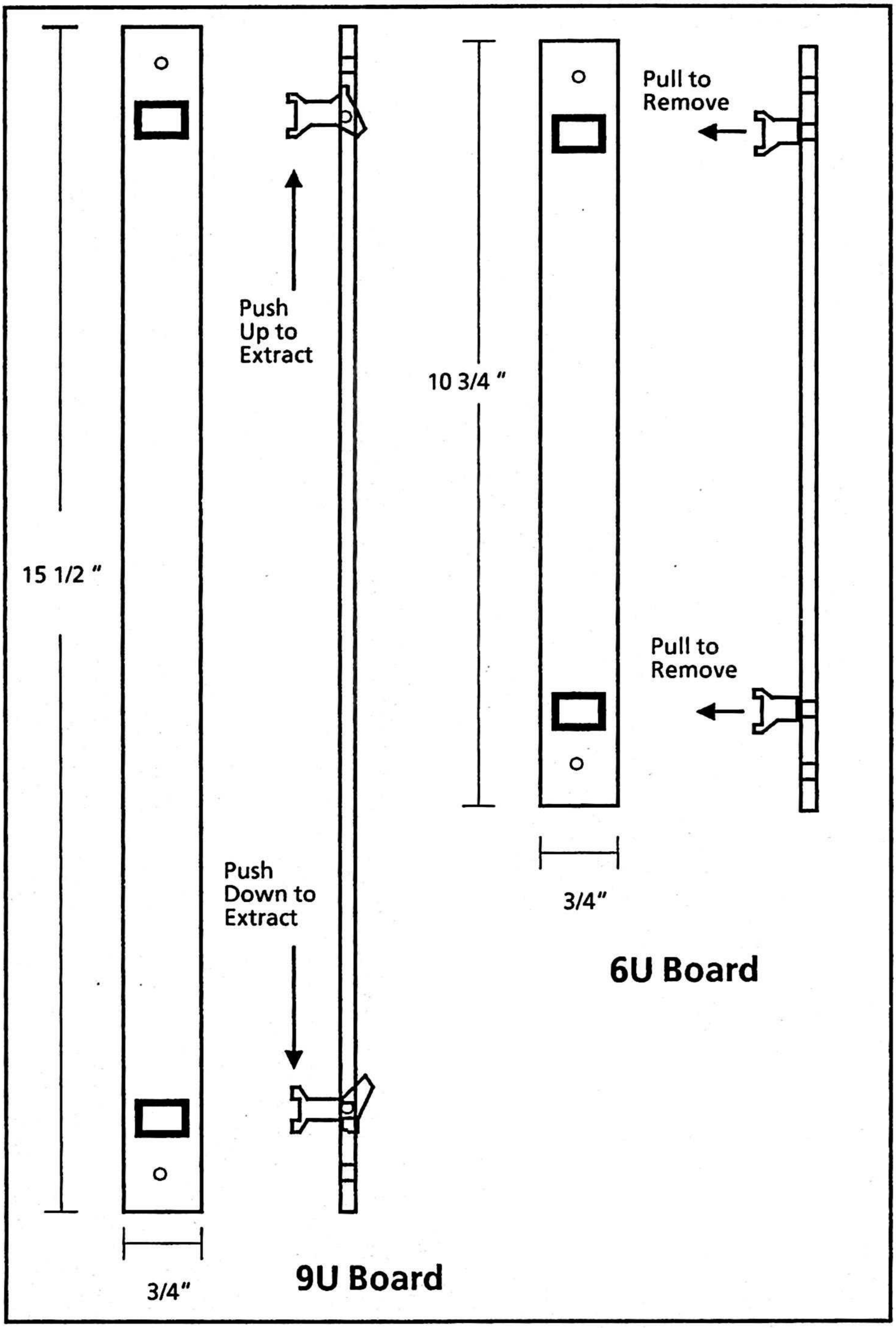

15 1/2 "
Push
Up to
Extract
Push
Down to
Extract
3/4"
9U Board
10 3/4 "
Pull to
Remove
Pull to
Remove
3/4"
6U Board

Figure 4-47. 6U and 9U Circuit Board Installation.

4.9.4 REMOVAL/INSTALLATION OF 9U CIRCUIT BOARDS

The 9U circuit boards of the SCRIBE system are the Display & Cursor Board, the BMPU Board, the Frame Buffer Boards, the Sync Gen Board) These 9U boards all share the same type of mounting hardware.

To remove any of these boards, follow this procedure.

Step 1: Refer to Figure 4-47. Locate the small slot-head screws at the top and bottom of the board's mounting panel.

Step 2: Loosen the slot-head screws that secure the board. These screws are the half-thread variety, so they will not come loose from the board itself.

Step 3: Grasp the extractor handles at the top and bottom of the board's mounting panel. These handles also act as levers for releasing the board. Gently push the top extractor handle up, and the bottom extractor handle down, to release the board. Then, pull both handles straight out from the chassis.

Step 4: Carefully remove the board from the mainframe. Be especially careful not to damage the board edges and corners during handling.

To install a 9U board, reverse this procedure.

4.9.5 REMOVAL/INSTALLATION OF VIDEO ENCODER BOARD

The Video Encoder board of the SCRIBE system is located on the inside of the mainframe's rear door. The board is mounted using either nylon stand-offs or threaded hardware. There are numerous cables connected to the Video Encoder board, so these must be labeled with great care to simplify re-installation.

To remove the Video Encoder Board, follow this procedure.

Step 1: Label each Encoder Board cable with its destination using tape-on labels or indelible ink. When complete, check the labels for accuracy.

Step 2: After you've checked the labels for accuracy, remove the cables from the Encoder Board. Be careful not to damage the cable or its connectors.

Step 3: Locate and release the nylon standoffs (or threaded hardware) that secures the board. (Refer to Figure 4-48.) To release the nylon standoffs, squeeze each standoff with needle-nose pliers while pulling up on the circuit board. When all standoffs are released, remove the board from the unit.

To re-install the Video Encoder Board, reverse this procedure.

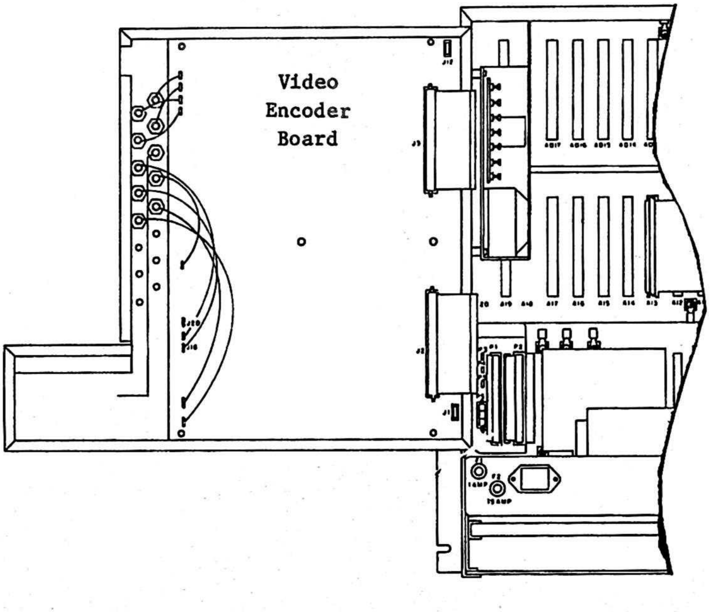


Figure 4-48. Video Encoder Board Installation

4.9.6 DISK DRIVE MODULE REMOVAL/DISASSEMBLY

The Disk Drive Module contains up to two floppy disk drives, one Winchester-type hard-disk drive, and a disk controller board. (Various versions of this module have different equipment. However, the physical installation for all versions is essentially identical.)

4.9.6.1 Disk Module Removal. To remove the Disk Drive Module from the SCRIBE mainframe, follow this procedure:

Step 1: Open the SCRIBE front panel. Locate the Disk Drive Module (refer to Figure 4-49).

Step 2: Open the SCRIBE rear panel. Locate the CPU Transition Board.

Step 3: Remove the CPU Transition Board from the rear of the chassis. Follow the 6U board removal instructions (paragraph 4.9.3).

Step 4: Locate the 50-pin header connector and ribbon cable at J3 on the Transition Board. Label the header connector with proper polarity and location, then remove the header.

Step 5: Re-secure the CPU Transition Board to the chassis.

Step 6: Locate the 4-wire power supply cable that runs between the power supply and the Disk Drive Module. This cable has an in-line connector which is located near the power supply, and is accessible through the SCRIBE rear door. Label and disconnect this cable.

Step 7: At the Disk Drive Module, locate four 6-32 screws and washers on the top left and top right edges of the module (shown in Figure 4-49). These four screws are used to secure the module into the mainframe.

Step 8: Being careful not to drop or lose the screws, remove the four screws securing the Disk Drive Module.

Step 9: Carefully slide the Disk Drive Module out of the chassis. Avoid damaging the 50-line ribbon cable and the 4-wire power cable as you remove the disk drive module.

Step 10: Place the Disk Drive Module on a clean, level surface for further disassembly.

To re-install the Disk Drive Module, reverse this procedure.

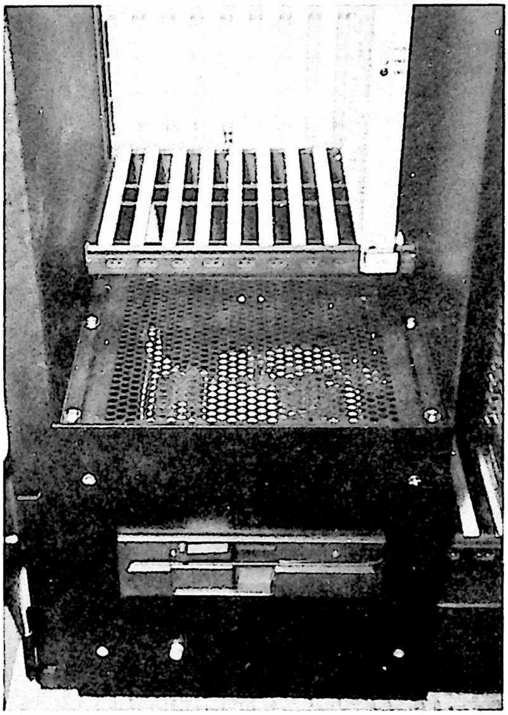


Figure 4-49. Disk Drive Module, Location and Mounting

4.9.6.2 Disk Drive Module Disassembly. To disassemble the Disk Drive Module, follow this procedure.

CAUTION

Components of the Disk Drive Module can be damaged by physical shock or by static discharge. Take all precautions against physical shock or static discharge while working on the Disk Drive Module!

Step 1: Refer to Figure 4-50. Locate the four 6-32 screws and washers that secure the module's top grating. (These screws are located on the sides of the module chassis.) Remove these screws, then remove the top grating. Save the screws and washers for re-assembly.

Step 2: Locate and remove the four 6-32 screws that secure the front panel of the Disk Drive Module, then remove the front cover. Save the screws and washers for re-assembly.

Step 3: Refer to Figure 4-50. Locate the four 6-32 screws and washers that secure the back cover of the module, and remove the back cover. Be careful not to damage the ribbon and power cables when removing the back cover. Save the screws and washers for re-assembly.

Step 4: Refer to Figure 4-51. Become familiar with the layout of the cables that connect the disk drives with the disk controller board (located at the bottom of the module). Using tape-on labels or indelible ink, label each cable connector with its polarity and destination.

Step 5: Be sure that the two cables going to the floppy disk drive(s) are properly labeled. Remove the cables from the floppy disk drive(s) as shown in Figure 4-52.

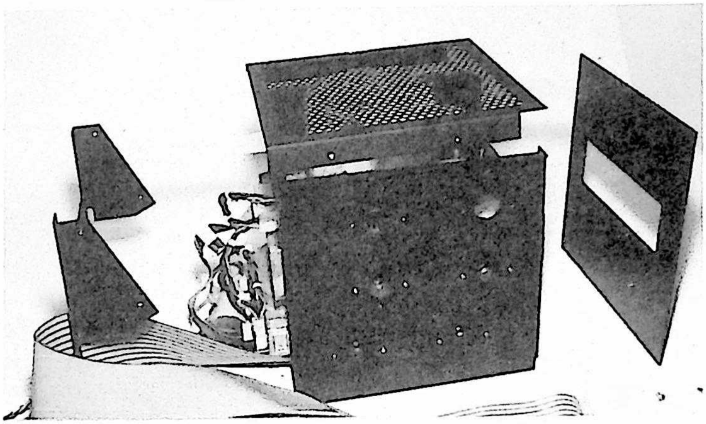


Figure 4-50. Disk Drive Module: Top Grating, Back Cover Removal

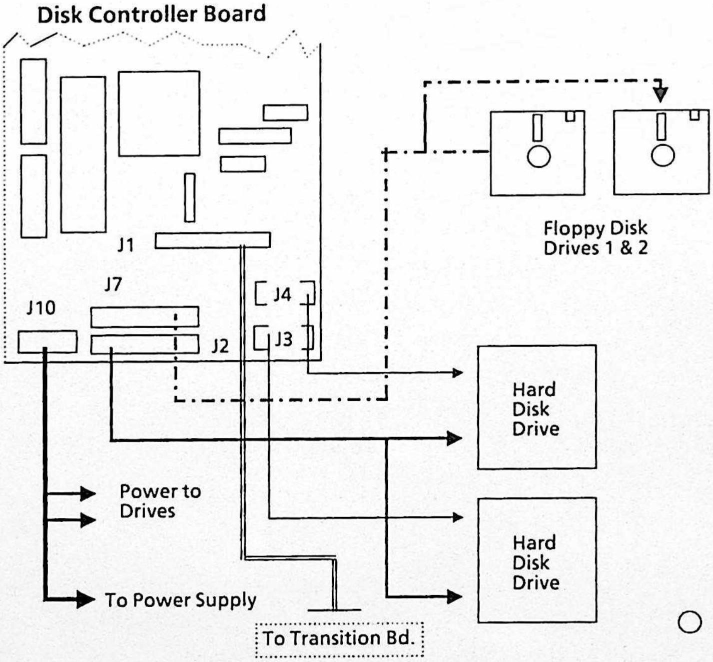

Disk Controller Board
J1
J7
J10
J2
J4
J3
Floppy Disk
Drives 1 & 2
Hard
Disk
Drive
Hard
Disk
Drive
Power to
Drives
To Power Supply
To Transition Bd.

Figure 4-51. Disk Drive Module. General Cabling Diagram

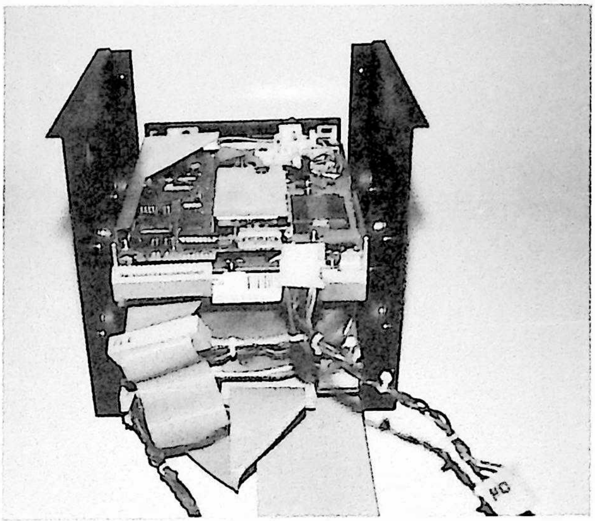


Figure 4-52. Disk Drive Module: Floppy Disk Drive Cable Removal

Step 6: Refer to Figure 4-53 and Figure 4-54. Locate the rubber shock mountings for the floppy disk drive(s). In the center of each shock mounting, there is a 4-40 screw. Remove the screws from the center of the shock mountings for each floppy disk drive. NOTE: It is not necessary to remove the rubber shock mountings when removing the disk drives!

Step 7: Being careful not to cause damage, lift each floppy disk drive free of the module. Save the screws and washers for re-assembly.

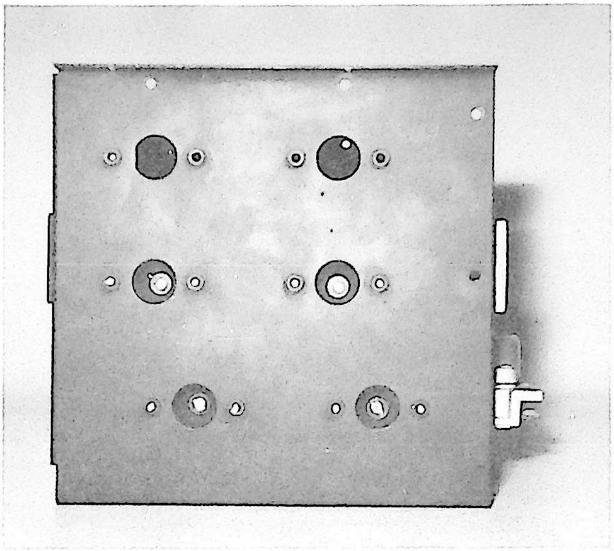


Figure 4-53. Disk Drive Module: Shock Mountings

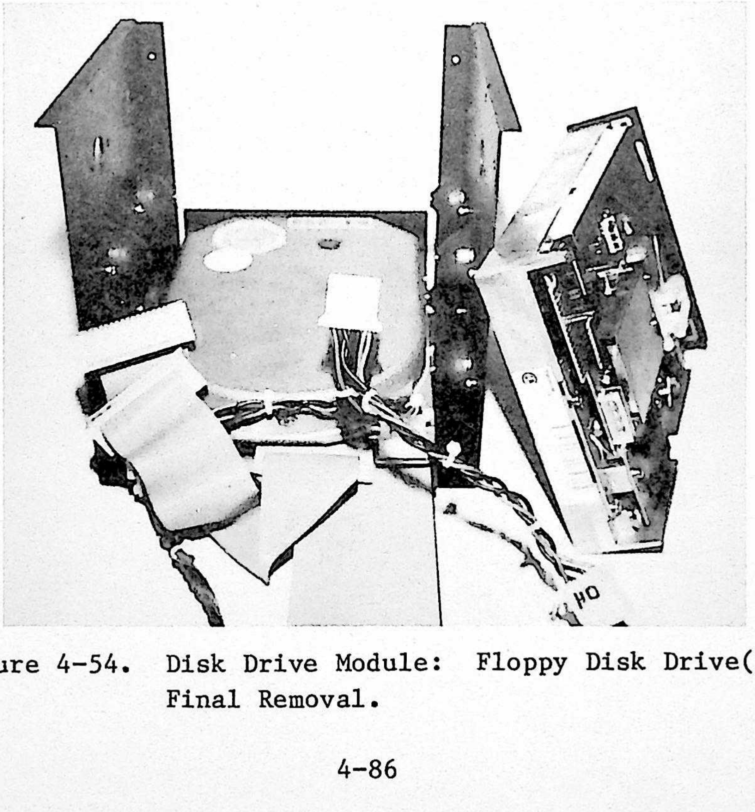


Figure 4-54. Disk Drive Module: Floppy Disk Drive(s), Final Removal.

Step 8: Be sure that the three cables (one 34-line ribbon, one 20-line ribbon, one 4-wire power) that connect the hard disk drive to the disk controller are properly labeled with location and polarity. Remove these cables from the hard disk drive as shown in Figure 4-55.

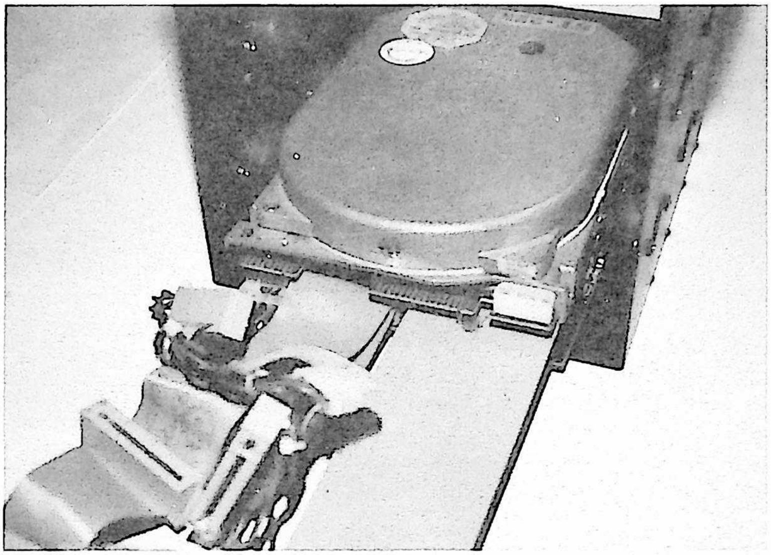


Figure 4-55. Disk Drive Module: Hard Disk Drive Cable Removal

Step 9: Refer to Figure 4-53 (DDM: Shock Mountings). Locate the four 6-32 screws that secure the hard disk drive to the rubber shock mountings. Being careful to support the hard disk drive, remove the four screws.

Step 10: Being careful not to subject the hard disk drive to physical shock, remove it from the Disk Drive Module (Figure 4-56).

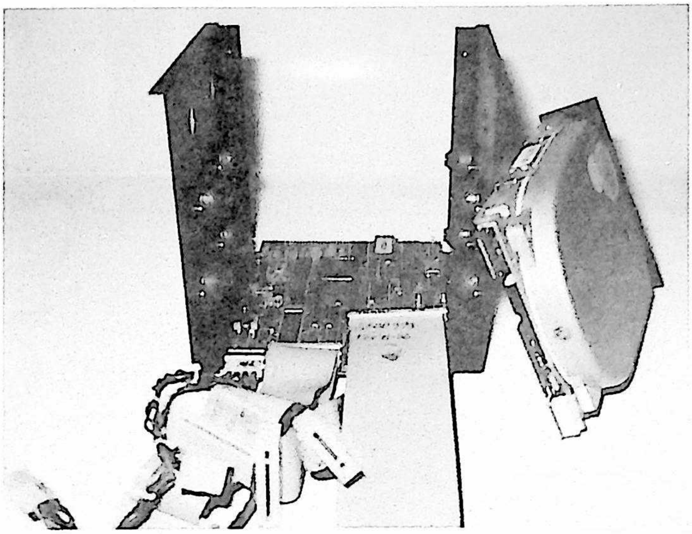


Figure 4-56. Disk Drive Module: Hard Disk Drive Final Removal

Step 11: Refer to Figure 4-57. Locate the Disk Controller Board, which is secured to the floor of the Disk Drive Module.

Step 12: Refer to Figure 4-58 (Disk Controller Cabling Diagram). Using Figure 4-58 as a guide, label all cable connections on the Disk Controller Board with their polarity and location.

Step 13: Be sure that all connectors are properly labeled. Then, remove the connectors from the Disk Controller Board, being careful not to damage the board or connectors.

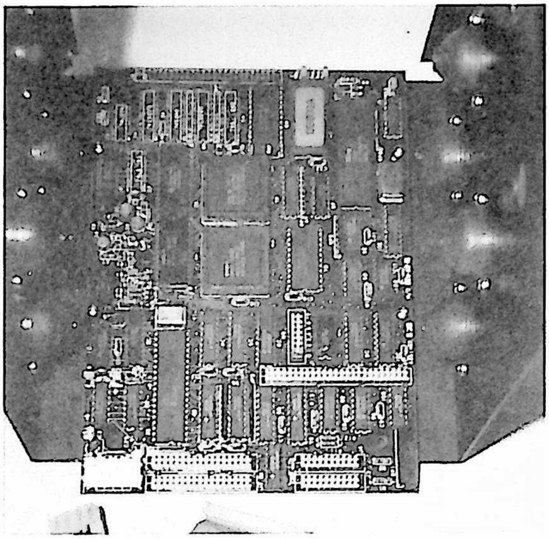


Figure 4-57. Disk Drive Module: Disk Controller Board

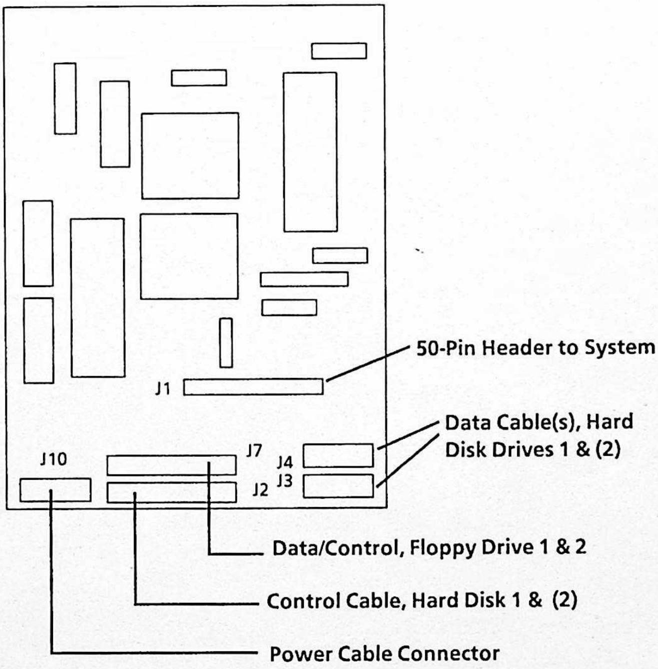

50-Pin Header to System
J1
Data Cable(s), Hard Disk Drives 1 & (2)
J10
J7
J4
J3
J2
Data/Control, Floppy Drive 1 & 2
Control Cable, Hard Disk 1 & (2)
Power Cable Connector

Figure 4-58. Disk Drive Module: Disk Controller Board Cabling Diagram.

Step 14: Refer to Figure 4-59. Locate the four 6-32 mounting screws and washers that secure the Disk Controller Board to the floor of the Disk Drive Module. Carefully remove these screws, being careful not to damage the board. Save the screws and washers for re-assembly.

Step 15: Carefully lift the Disk Controller Board out of the Disk Drive Module.

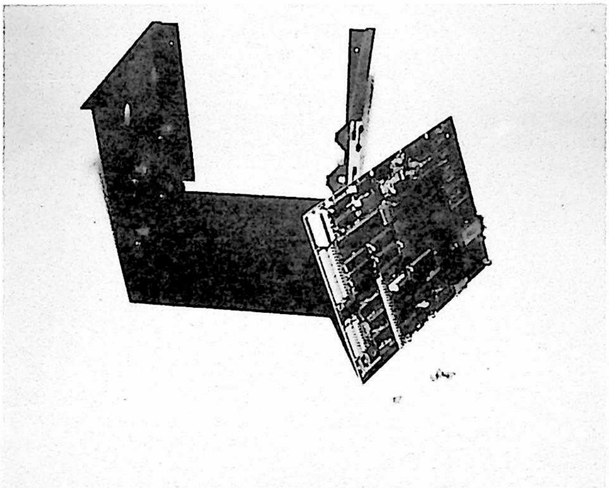


Figure 4-59. Disk Drive Module: Final Disassembly.

This concludes the Disk Drive Module disassembly procedure. To re-assemble the Disk Drive Module, reverse this procedure.

4.10 SHIPPING INSTRUCTIONS

This paragraph describes how to arrange to ship boards and subassemblies of the SCRIBE system and how to pack these properly for trouble-free shipping.

CAUTION

You must obtain a Material Return Authorization number (MRA number) before you ship any equipment to CHYRON for repair. If you do not obtain authorization, your equipment will be returned to you at your cost and delay!!

To obtain a MRA, contact the CHYRON MRA department, at 5 Hub Drive, Melville, NY; or call (in the U.S.) 516 249-3018.

4.10.1 PACKING GUIDELINES

Boards must be securely packed before shipment. **REMEMBER!!! IT IS BETTER TO USE A BOX THAT'S A LITTLE BIG THAN TO USE A BOX THAT'S A LITTLE SMALL!!!**

Enclose boards in static-resistant plastic envelopes and/or ttake other precautions against static discharge. Use a lot of schock-absorbing packing material, such as styrofoam peanuts or foam-rubber blocks, to protect the boards. Be careful to protect the edges of all boards!

Seal each box with sturdy filament packing tape. (It's better to use too much tape than too little...) Seal the box well enough to withstand rough handling. Mark each box "ELECTRONIC EQUIPMENT--- FRAGILE!"

4.10.2 GENERAL SHIPPING INSTRUCTIONS

Contact the CHYRON customer service department for an MRA, and for any other shipping information. The address is CHYRON CORPORATION, Customer Service Department, 5 Hub Drive, Melville, NY 11747. The telephone number is (516) 249-3018.

Send boards by registered/insured mail, UPS, or insured overnight carrier. It's best to check with CHYRON for the safest, most effective shipping method.

Feel free to contact the CHYRON Customer Service Department with any questions, or for any additional information.

4.11 SCRIBE DIAGNOSTICS ERROR RESPONSES

The SCRIBE diagnostics generate error responses to describe errors encountered during testing. These error responses and definitions are listed alphabetically in this paragraph. For more information about a particular error response, please contact CHYRON Customer Service for assistance.

An illegal address was tested	CPU Test has a memory addressing problem.
Bad FAIL LED	Fail LED does not light during CPU FAIL LED test.
BMPU did NOT return an acknowledge to CPU.	BMPU did not send IACK* to CPU within three seconds of CPU poll.
BMPU ERROR CONDITION	Error encountered when BMPU returns a fail vector to the CPU. (If BMPU detects an error during internal tests, it generates a fail vector.)
BMPU FAILED TO INTERRUPT WITHIN 3 SECONDS	An interrupt was expected from the BMPU, none occurred within three-second timeout limit.
Bus Error	Non-specific bus error. To recover, reset and re-boot system.
Bus Error occurred at $	Non-specific bus error, with address where error occurred. To recover, reset and re-boot system.

SCRIBE DIAGNOSTICS ERROR RESPONSES, continued

Bus error occurred during test	Non-specific bus error during CPU clock/timer tests.
Can not clear MCR fail bit	CPU fail light will not clear due to stuck bit of MCR.
Can not deselect MCR parity enable bit	<----- Parity errors --->associated with CPU Parity tests
Can not deselect MCR parity incorrect parity bit	<-----
Can not disable PTM interrupts	CPU's PTM interrupts are not disabled on command.
Can not disable SCSI interrupts	The SCSI Interrupts bit won't reset in the MCR register.
CAN NOT OUTPUT TO PROMPT MONITOR	CPU polls Display & Cursor board and looks for DTACK*. If no DTACK* is received, CPU assumes there is no Display & Cursor board in system. Check board seating and connections.
Can not select MCR parity enable bit	<------ Parity errors associated with CPU Parity tests
Can not set MCR fail bit	CPU test cannot force a failure due to stuck bit in MCR.

Configuration # indicated a 68881, but it was not detected.	The CPU configuration number specifies a co-processor chip but test shows none present. Check for damaged 68881 chip.
DATA EXPECTED -> $ DATA RETURNED -> $	Response to error in write/read memory test.
Day did not change to 1	CPU Real-Time Clock Rollover error messages
Tens Year did not change to 0	
Unit Year did not change to 0	
Tens Month did not change to 1	
Unit Month did not change to 1	
Tens Day did not change to 0	
Unit Day did not change to 1	
Tens Hour did not change to 0	
Hour did not change to 0	
Tens Minute did not change to 0	
Unit Minute did not change to 0	
Tens Sec did not change to 0	
Unit Sec did not change to 1	
Did not get an abort interrupt	CPU Abort button test; if the button was not pressed within three seconds, OR if button was pressed and no interrupt occurred within three seconds, this error message appears.
Did not receive an interrupt	No interrupt generated when one was expected.
Did not set Composite Interrupt flag	An interrupt was received from the PTM, but the CPU did not set the Composite interrupt flag.

SCRIBE DIAGNOSTICS ERROR RESPONSES, continued

Disabled MCR WIP, but got parity error	<------ Parity errors associated with CPU Parity tests
Error Code = \$	Error Code for Clock/Timer.
Error Status Code -> determine failure.	Status code allows you to

Error Status Code is generated as two pairs of hex values. There are two columns of values below; the first hex pair corresponds to the first column, and the second hex pair corresponds to the second column.

Error Status Code -> \$XX XX

	First Hex Pair		Second Hex Pair
0	Rx Character Available	0	All Sent
1	Zero Count	1	Residue Code 2
2	Tx Buffer Empty	2	Residue Code 1
3	DCD	3	Residue Code 0
4	Sync/Hunt	4	Parity Error
5	CTS	5	Rx Overrun Error
6	TX Underrun/EOM	6	CRC/Framing Error
7	Break/Abort	7	End Of Frame/(SDLC)

Errors were found to occur in the following: Failed	This message is output when a failure occurs during Font Memory testing, indicating banks of memory that failed during the test.

SCRIBE DIAGNOSTICS ERROR RESPONSES, continued

FAILING BMPU ADDRESS = $	Response after BMPU error, and location.
Failed at $ Data Written: $ Data Read: $	Failing address location, and data written and read during write/read memory test.
Font Memory Error Condition	BMPU tests Font Memory, and BMPU encounters a Font Memory memory error.
Font Memory Error Condition Found using VME bus Error Address = $	Font Memory error during BMPU write/VME read, and location.
FONT MEMORY PARITY ERROR ON VME U#	Font Memory testing has encountered a parity error while testing over VME bus, at the specified U#.
FONT MEMORY PARITY ERROR ON VMX U#	Font Memory testing has encountered a parity error while testing over VMX bus, at the specified U#.
Frame Buffer Error Condition Found Using VME Bus	Frame Buffer error during BMPU write/VME read.
Frame Buffer Memory Error Condition	BMPU tests Frame Buffer, and Frame Buffer does not return a DTACK*; or BMPU encounters a memory error.
Frame Buffer Memory Error Condition Found Using VME Bus	BMPU tests Frame Buffer memory; verification by CPU found a data error.

SCRIBE DIAGNOSTICS ERROR RESPONSES, continued

HIT R TO RESTART DIAGNOSTICS	Allows you to restart diagnostics after BMPU fail condition.
Incorrect Interrupt Level Generated for Parity Test	During Font Memory parity logic interrupt test, Font Memory outputs wrong interrupt level.
Incorrect parity did not cause a bus error	<----- Parity errors associated with CPU Parity tests
Incorrect system configuration found, REBOOT system.	CPU address $F4400D contains system configuration; including size of on-board memory, presence of 68881 co-processor, etc. This message is generated when an inconsistency occurs between tested configuration and configuration table, requiring reboot.
Interrupt Flag not set in RTC status register	External port read CPU Real-Time Clock status register: interrupt flag expected but not detected.
Interrupt has occurred but there was an ERROR	Keyboard Test error. Keyboard interrupt(s) not generated properly. Status code allows you to determine failure.

SCRIBE DIAGNOSTICS ERROR RESPONSES, continued

MAP RAM LOAD ERROR	BMPU loads MAP RAM from disk. Same data is loaded into CPU RAM for comparison. If comparison fails, this message is output.
MEMORY ERROR HAS OCCURRED, OUTPUT ERROR LOG? ENTER Y OR N	Error encountered during Font Memory or Frame Buffer tests; allows you to output error log for failing addresses.
MSR parity error flag will not reset	Parity errors associated with CPU Parity tests
MSR parity error flag will not set	
NO FONT MEMORY FOUND	During Font memory test, the CPU checks for banks of memory by polling and reading DTACK*. If a non-existent bank is polled, this message is generated.
Note: PARITY is DISABLED Note: PARITY is ENABLED	During Font Memory tests, these messages indicate whether Font Memory is configured with parity enabled or disabled.
NOTICE - Size does NOT match configuration	The system has detected a mismatch between tested size of CPU CMOS RAM and size specified in Configuration Table.

SCRIBE DIAGNOSTICS ERROR RESPONSES, continued

NOTICE - Tested SCSI chip, but configuration # indicated no chip should be present.	CPU configuration error. Test SCSI operation through SCSI diagnostics.
OUTPUT THE ERROR ADDRESS LOG? ENTER Y OR N	Error encountered during Font Memory or Frame Buffer tests; allows you to output list of suspect addresses and chips.
Read incorrect Data at $	------> Parity errors associated with CPU Parity tests
Received parity error while writing $ with Data of $	Error during memory test with parity; provides address of error and data written to that address.
RUN DISPLAY VME INTERFACE TEST AGAIN	If during the background palette and palette memory tests a bus error occurs, this message is generated. This means that an address was attempted by the CPU and no DTACK* was returned. Running the VME Interface test will ensure that the interface to the VME bus is functioning properly and that the error occurred for another reason.

SCSI bus in illegal state, check fuse (F1)	F1 is a fuse on the CPU board between P1 and P2. If this message occurs, or when there is any SCSI problem that is not explainable through testing, check this fuse. (Refer to Section 6 of this manual.) When there is a disk subsystem problem, check the cables between the CPU board, the CPU Transition board, and the Disk Drive chassis. Then, be sure to check fuse F1 on the CPU board for continuity. Do these things BEFORE dismantling the Disk Drive chassis!!!
SCSI chip not detected, but Configuration # indicates a chip.	Configuration # indicates SCSI chip; but chip does not return a DTACK* to the CPU when tested.
Serviced too many PTM interrupts	PTM is interrupting more frequently than specified interval.
Test had a Bus Error	Non-specific bus error occurred during SCSI test.
The following chips are SUSPECT:	Memory errors found at specific chips. Also, the system will output the number of errors per chip, IN HEX.

Timer failed to generate an interrupt	CPU clock was set to generate an interrupt; if no interrupt is detected, then the error is posted.
Timer failed with Internal Clock Timer failed with External Clock	CPU timer is checked against system clock. If one is not in sync with the other, one of these errors occurs.
TRAP ERROR. HIT RESET AND RESTART DIAGNOSTICS	Fatal error was encountered during testing (ie: bus error, zero divide, etc.), requiring program restart.
Unable to read SCSI registers in Test Mode	SCSI chip has an internal Test Mode; CPU is unable to read or write to SCSI during test mode, indicating an error.
Unable to reset SCSI device by the MCR	SCSI chip will not reset through Module Control Register action, indicating an error.
WARNING - Redundant Addressing above 128K, check J2 & U98.	The system checks for size of RAM and then checks for the correct addressing. If there is a redundancy, this indicates address-decoding problems. Check connector J2 and chip U98.
WCS RAM LOAD ERROR	BMPU loads WCS RAM from disk, WCS data is also loaded into CPU RAM, and compared with data in WCS RAM on BMPU. If comparison fails, this message is output.

Section 5

SCRIBE VIDEO ALIGNMENT PROCEDURES

5.1 INTRODUCTION

The SCRIBE video sections (sync generator, encoder, keyer/fader) are completely aligned at the factory before shipment. However, the SCRIBE may occasionally require minor internal adjustments to ensure proper operation. This video alignment procedure allows the technician to completely align the SCRIBE sync generator, encoder, and keyer sections.

5.2 GENERAL INFORMATION

This alignment procedure is set up in a step-by-step format. Adjustment locations are numbered in the procedure, and are called out in component layout diagrams. (See Figures 5-1 and 5-2, at the end of theis section.) The alignment procedures cover both NTSC and PAL versions. Differences between NTSC and PAL are covered as they are encountered in the procedure.

There are several minor variations between earlier and more recent encoder boards. Such variations are also covered as they are encountered in the procedure.

If you have any questions about this procedure or about the equipment or test setup, please contact CHYRON Customer Service by phone or letter for more operation.

5.3 EQUIPMENT REQUIRED

The following equipment is required in order to properly complete this alignment procedure.

+5, +12, -12 volt power supply
Oscilloscope w/2 probes
Frequency Counter w/one probe
BNC - Chabin adapters (4)
Color Video Monitor (PAL or NTSC)
B&W Video Monitor (PAL or NTSC)

Video Generator: NTSC (Tektronix 1910 or equivalent)
PAL (Tektronix 1411 or equivalent)

Vectorscope: NTSC (Tektronix 520A or equivalent)
PAL (Tektronix 521A or equivalent)

Waveform Monitor: NTSC (Tektronix 1485 or equivalent)
PAL (Tektronix 1485R or equivalent)

5.4 SYNC GENERATOR BOARD ALIGNMENT

Step 1. Remove the Sync Generator Board (P/N 6A10690) from the SCRIBE chassis. At the test bench, connect P3 of the Sync Gen board [1] to J20 - 3 of the Analog Transition board (located on the SCRIBE backplane). Connect +12 and -12 volts to P6 on the Analog Transition board. Connect the video generator output to P3 on the Analog Transition board. Connect +5 volts to the 5v side of C130 [2]. Be sure to observe the note on the component layout and locations diagram.

Step 2. Attach one oscilloscope probe to TP2 [3]. Check for a clean 6 volt ± 0.2v signal. If voltage is not within this range, adjust C29 [4]. Any large spikes can be minimized by adjusting R20 [5].

Step 3. Attach frequency counter probe to TP4 [6]. Check for a 14.318 MHz signal (PAL: 17.735 MHz). If off frequency, adjust C29 [4].

Step 4. Attach frequency counter probe to TP3 [7]. Check for a 3.58 MHz signal (PAL: 4.43 MHz). If off frequency, adjust R6 [8].

Step 5. Attach frequency counter probe to TP1 [9]. Check for 15.734 KHz (REF H) signal (PAL: 15.625 KHz). While monitoring frequency, disconnect and reconnect the genlock source (video generator). The frequency at TP1 should not change. As a second check, attach an oscilloscope probe to TP1. When the genlock source is removed, the signal at TP1 should invert. While the genlock source is connected, CR1 [10] should be lit. When the source is removed, CR1 should go off.

Step 6. Attach scope probe to TP18 [11] (under small plug-in oscillator board). Check for a clean signal at approximately 5V. If off voltage, adjust C1 [12] on the small oscillator board. Attach frequency counter probe to U47, pin 3 [13]. Check for 24.3 MHz signal. If off frequency, adjust C1 [12] on oscillator board. Recheck voltage at TP18 [11].

Step 7. Attach frequency counter probe to U47, pin 5 [13]. Check for 12.15 MHz signal.

Step 8. Attach scope probe to U65, pin 5 [14]. Signal should be positive-going H sync pulses every 64 microseconds.

Step 9. Set scope to CHOP. Attach one probe to the genlock video input at pin 2 of P3 on the ATB. Attach second probe to R171 [15] and insure this signal is genlocked to the input signal (does not drift).

Step 10. Attach P4 of the ATB to the wave form monitor. Adjust R4 [16] for minimum signal. Adjust R5 [17] for minimum signal. Resultant should be sync at -40 IRE, burst, and blanking at 0 IRE.

Step 11. Attach scope probe to C140 [18]. Confirm presence of unterminated video signal. Move scope probe to emitter of Q19 [19] and check for luminance signal. Move probe to emitter of Q16 [20] and check for signal that is chrominance only.

Step 12. Attach scope probe to TP7 [21]. Check for 5Vp-p, negative-going pulses.

Step 13. Attach scope probe to TP8 [22]. Check for negative-going REF V pulses. If not seen, adjust R20 [5] until they appear.

Step 14. Attach P5 to waveform monitor. Expand to maximum magnification and examine leading edge of sync. There should be no jitter. Adjust C132 [23] for no jitter and squared sync pulse without appreciable overshoot. Set wavefrom monitor to 2 Field. Adjust R20 [5] for proper vertical phasing.

5.5 ENCODER BOARD ALIGNMENT

Step 1. Attach scope probe to R9 [2]. One side should have blanking signals, the other side should be to ground. Move probe to R10 [3]. One side should have sync pulses, the other side ground. Move probe to R11 [4]. One side should be at 5V, the other side to ground.

Step 2. Attach scope probe to J16, pin 2 [5]. Check prompt video for proper signal levels. Expand trace and adjust C4 [6] for best rise time with no overshoot.

Step 3. Attach scope probe to TP12 [7]. Check for 1V signal.

Step 4. Attach scope probe to emitter of Q26 [8]. Check for R signal--square wave, 0-1V, 2 highs per line. Move probe to emitter Q34 [9] to check for G signal--square wave, 0-1V, 1 high per line. Move probe to emitter of Q44 [10] to check for B signal--square wave, 0-1V, 4 highs per line.

Step 5. Attach scope probe to R330 [11]. Check for luminance signal, 0 to -3V. Attach second probe to R364 [12] and set scope to CHOP. R364 should have a 1 Vp-p inverted video signal. Also check for 250 nanosecond delay between signals.

Step 6. Attach scope probe to R366. Check for 0 to -1V signal.

Step 7. Attach scope probe to R375 [14] and expand scope to examine falling edge of signal. Adjust L13 [15] and L14 [16] simultaneously to achieve best pulse shape with a minimum of overshoot and undershoot, and a fall time of 140+/-15 nanoseconds.

Step 8. Attach scope probe to collector of Q55 [17]. With J15 [18] removed, a luminance signal should be seen. Attach jumper between pins 1 and 2. Ground potential should be seen. Attach jumper between pins 2 and 3. Go to switch #2 of the 4-switch DIP switch on the front of the Sync Generator Board. Turn switch ON. Luminance signal should be seen. Turn switch OFF. Ground potential should be seen. Restore switch to ON position.

Step 9. Attach scope probe to emitter of Q54 [19]. A 0 to -500mV luminance signal should be seen.

Step 10. Attach scope probe to TP5 [20]. An 800mVp-p U signal should be seen. Adjust R230 [21] to insure white line is perfectly straight. Adjust R232 [22] for proper burst level. Expand scope and examine any of the rising edges of the signal. Adjust L1 [23] and L2 [24] simultaneously for 300 +/- 15 nsec rise time with no overshoot.

Step 11. Attach scope probe to TP11 [25]. A 1.2Vp-p V signal should be seen. Adjust R23 [26] for straight white line. Expand scope and examine any of the rising edges of the signal. Adjust L6 [27] and L7 [28] simultaneously for 300 +/-15 nsec rise time with no overshoot.

Step 12. Attach one scope probe to TP6 [29] and check for subcarrier signal. If not there, confirm that switch #3 of the 4-switch DIP switch on the front of the Sync Generator Board is OFF. Subcarrier signal should be 1 VP-p. Attach second probe to R259 [30] and set scope to CHOP. Check second signal is 300 mVp-p subcarrier signal. Expand scope and confirm that the signal at R259 [30] is leading the signal at TP6 by 90°. Adjust R221 to insure this.

Step 13. Attach scope probe to R212 [32]. Check for 250-300 mVp-p signal. Move probe to emitter of Q41 [36]. Check for chroma signal.

Step 14. Attach Video 1 Out [37] to the waveform monitor. Select Color Bar input from the Video Generator and confirm color bar output at the waveform monitor. Adjust R370 [38] for blanking at 0 IRE (DC offset). Adjust R369 [39] for -40 IRE sync level. Adjust R354 [50] for pedestal at 7.5 IRE. Expand trace to 1 microsecond/division. Adjust J5, Sync Timing, and R21 and R22, Burst Delay and Burst Timing (on Sync Generator Board) for proper horizontal signal timing. Fully expand magnifier on monitor. Adjust R211 [42] and R288 [41] simultaneously to minimize residual subcarrier, resulting in the smoothest signal possible. Move H position on monitor until white bar is reached. Attach a jumper between pins 1 and 2 of J15 to turn on the notch filter. Adjust C151 [44] for the smoothest signal with the least amount of overshoot. Adjust R230 [21] and 231 [26] simultaneously to minimize residual subcarrier. Move Video 1 Out from waveform monitor to vectorscope. Adjust R190 [45] and 257 [46] for correct chroma amplitude, and R221 [31] for correct quadrature insuring that the chroma dots fall into their correct boxes. Adjust R232 [22] for 100% burst. Reattach output to waveform monitor, expand trace, and locate white bar. Readjust R230 [21] and 231 [26] for minimum residual subcarrier. Reset monitor to normal trace and adjust R368 [47] so white bar peaks at 100 IRE.

Step 15. Move output from Video 1 Out to Video 2 Out [49] and insure signal is correct. Move output to Color Edit Out and insure that signal is correct.

5.6 PROGRAM/PREVIEW MIXER ADJUSTMENTS (on Encoder Board)

Install Encoder, Analog Transition, and Sync Generator boards into the Scribe. Connect all back panel BNC-Chabin which is to be connected from P3 on the Analog Transition Board to J20 (REF VIDEO IN) on the Encoder Board. Attach video generator to PROGRAM IN. Attach PROGRAM VIDEO 1 to the waveform monitor. Attach PROMPTS to a separate B/W monitor. Select Multipulse 100 IRE at video generator (NB: Color Bars with 100 IRE white may be substituted if Multipulse 100 unavailable.) Power up Scribe and create the following screen.

1. After message compose, load a Swiss font into the font memory (if such a font available--if not, load in an edgeless font with the least amount of serif). The Swiss 50 line font is #301. After font is loaded, type CNTL-B. Select the black square of the palette, enter 100 at the keypad (not the keyboard) and depress the space bar. Then select the white square of the palette, enter 200 at the keypad, and depress the space bar. Hit CNTL.

2. Move output to COLOR EDIT. Type CNTL-S. Refer to PROMPTS monitor. Type L to allow for a change in the left margin. Hit CLR at the keypad, then enter 1. Depress the left arrow key and move left margin until it is almost at the left screen edge. Hit CNTL, then HOME.

3. Move output to PROG VIDEO 1. Ensure program blanking level is at 0 IRE by adjusting R128, PGM DC OFFSET. Adjust R124, PGM GAIN, for -40 IRE and 100 IRE white level.

4. Type black captial's down the left side of the screen, one per line. Fully expand waveform monitor and move trace until first character is reached.

Adjust R293, DC OFFSET, for black level at 7.5 IRE. Adjust R295, GAIN, for program level trace to match black level, but before trace starts to clip (bottom will begin to flatten and widen when clipping). Adjust INSERT DC LEVEL, R158, to match 7.5 IRE and INSERT GAIN, R175, to match traces.

5. To match key rise time with program rise time, use the following:

    a. Jumpers J8-J11 are 80 nanosecond adjustments. They should be moved simultaneously to the same respective jumper position.

    b. Jumper J7 is a 40 nsec adjustment.
    c. Jumper J6 is a 5 nsec adjustment.
    d. R168 is a variable resistor.

Adjust all four in order listed to obtain best overlap signals.

6. Move output to PREV VIDEO. Adjust levels and width using R32, DC OFFSET, R31, PREV GAIN, R71, INSERT DC OFFSET, R70, INSERT GAIN, R63, WIDTH.

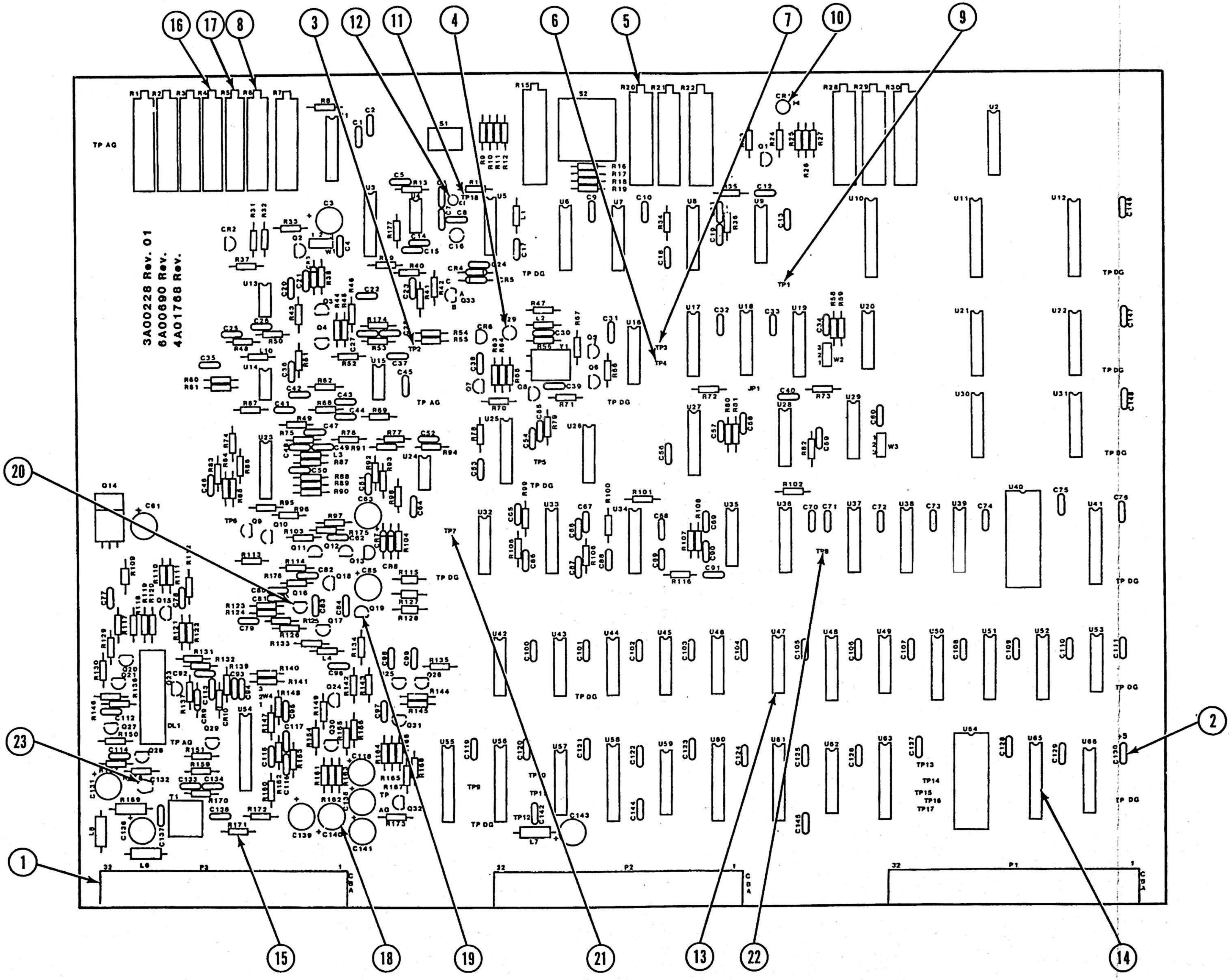
7. Move output to DLY KEY. Turn insert off by typing CNTL-1. Examine waveform:

Adjust L11 and L12 to achieve best symmetrical trace with no overshoot or undershoot. Turn insert on (CNTL-1) and move output to PROG VIDEO 1. Double check trace of character as in 5 and 6 and readjust if necessary.

8. Hit ERASE, then CNTL-B-ERASE-CNTL to clear screen of characters and backgrounds. Select color bars at video generator. Adjust C42, PGM HF, for proper chroma phase and amplitude if necessary. Create a color bar signal from Scribe by typing capital's (8 per color in Swiss 50) to match bars from video generator.

Adjust insert phase to match using: COARSE PHASE ADJUST, S2 on Sync Generator Board, FINE PHASE ADJUST, R15 on SGB, INSERT HF, C52 on Encoder board.

9. Move output to PREV VIDEO. Adjust C10, PVW HF, and C19, INSERT HF, for proper amplitude and phases.


16
17
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3
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11
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5
7
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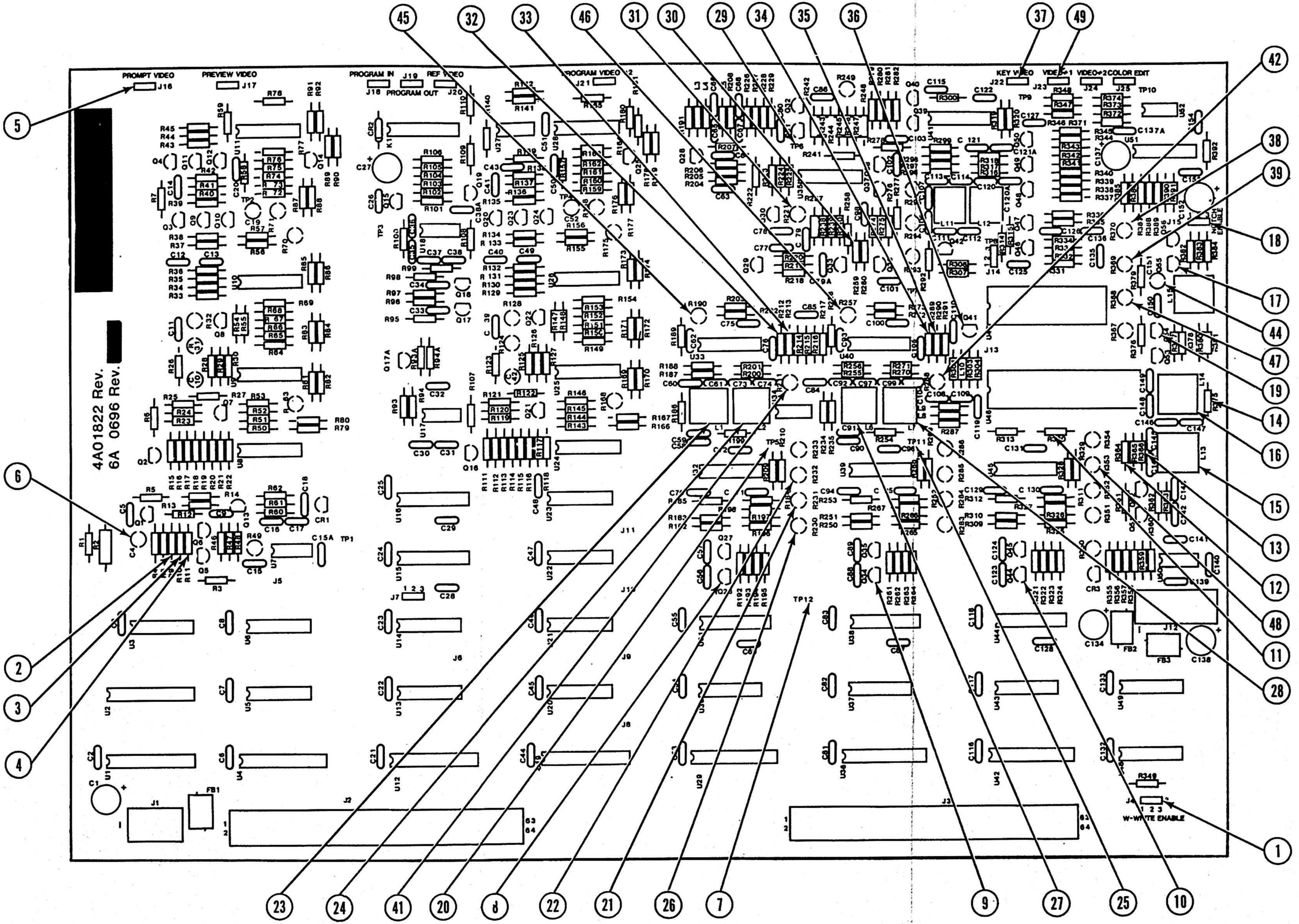
23
1
2
15
18
19
21
13
22
14
3A00228 Rev. 01
6A00690 Rev.
4A01768 Rev.
P3
P2
P1
TP AG
TP DG
TP1
TP2
TP3
TP4
TP5
TP6
TP7
TP8
TP9
S1
S2
DL1
T1
U64
U40

Figure 5-1. Sync Gen Bd. Adjustment Locations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10
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22
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20
41
24
23
5
6
2
3
4
PROMPT VIDEO
J16
PREVIEW VIDEO
J17
PROGRAM IN
J18
J19
PROGRAM OUT
REF VIDEO
J20
PROGRAM VIDEO 2
J21
KEY VIDEO
J22
VIDEO+1
J23
VIDEO+2
J24
COLOR EDIT
J25
TP9
TP10
J13
J14
J12
FB2
FB3
C134
C138
J11
J9
J8
J6
J7
J5
TP1
TP12
J1
FB1
C1
J2
J3
J4
W-WRITE ENABLE
4A01822 Rev.
6A 0696 Rev.

Figure 5-2. Encoder Bd.
Adjustment Locations
5-11/5-12

Section 6

ROUTINE MAINTENANCE PROCEDURES

6.1 GENERAL

This section provides operational maintenance procedures for the SCRIBE system. These procedures are to be performed periodically or as needed, as noted in the individual case.

These maintenance procedures, when followed regularly, will help to ensure trouble-free operation of your SCRIBE system.

This section contains a schedule for operational maintenance, instructions for replacing the back-up battery for the MVME117 CPU board memory/clock system, and instructions for modifying the SCRIBE Drive Configuration Table, which is a procedure required when installing or removing disk drives or disk controllers.

6.2 SCHEDULED MAINTENANCE

The following procedures should be performed at the intervals specified in Table 6-1 (below). These procedures require only standard tools and equipment. For more detailed diagnostic procedures, consult Section 4 of this manual.

Table 6-1. Operational Maintenance Schedule

Check external connectors for corrosion	(every six months)
Exterior cleaning	(every six months)
Check all internal hardware fasteners	(every six months)
Clean dust filters in chassis	(every six months)
Check board seating in card cage	(every six months)
Check internal video cable connections	(every six months)
Check internal ribbon cable connections	(every six months)
Check encoder for proper alignment	(every six months)
Check power supply voltages	(every six months)
Replace lithium cell on CPU board	(every thirty-six months)
Run system diagnostics (See Section IV)	(every six months)

Note

Special environmental conditions (such as excessively dry, damp, hot, or dusty environments) require more frequent scheduled maintenance on all items except for battery replacment.

6.3 SPECIAL MAINTENANCE PROCEDURES

6.3.1 REPLACING CPU BOARD LITHIUM CELL

Procedure for replacing Lithium Cell (BT1) on MVME117 CPU board:

CAUTION!

Please do NOT attempt to remove the battery unless you have adequate desoldering facilities, and you are familiar with soldering/desoldering procedures on multi-layer P.C. boards. Excess soldering heat can de-laminate the circuit board, resulting in board failure.

Step 1: Power down the SCRIBE. Open the unit's front panel, and locate the CPU board (which resides in Slot #1). Remove the two screws securing the board in place, and use the extractors on the top and bottom of the edge-card to remove the board.

Step 2: Locate jumper J5, which is near the square co-processor socket. Remove the jumper from J5.

Step 3: Locate lithium battery BT1, which is near the middle front edge of the circuit card, on the component side. Note the polarity of BT1.

Step 4: Carefully desolder the power leads and supports (two power leads, and two supporting leads) of BT1, and lift the battery away from the CPU board. Discard BT1.

CAUTION!

Be sure to insert the replacement BT1 in exactly the same position as the original battery. Failure to observe battery polarity may result in damage to the CPU board.

Step 5: Being careful to observe battery polarity, insert replacement battery BT1 into the previous BT1 location on the CPU board.

CAUTION!

Be careful not to over-heat the printed-circuit board material while soldering BT1 into place. Excess soldering heat can de-laminate the circuit board, resulting in board damage. Also, be careful not to use excess solder on the board which may cause solder bridges and board failure.

Step 6: Solder BT1 leads into place. Clip excess lead length on the non-component side of the board.

Step 7: Replace the jumper link at J5, which was removed in Step 1.

Step 8: Replace the CPU board in Slot #1 of the SCRIBE mainframe. Secure the board with the screws removed in Step 2.

Step 9: Power up the SCRIBE unit, and set the Real-Time clock. To test the new battery in the unit, power off the SCRIBE, and check for valid real-time clock data.

6.3.2 REPLACING FUSE F1 ON MVME117 CPU BOARD

The MVME117 CPU board has a subminiature fuse, which protects the SCSI subsystem from damage. If this fuse is blown, the SCSI subsystem will not be operational.

The Diagnostic program tests for this fuse through the CPU board tests. If this fuse appears to be blown, the system will prompt with: "SCSI port not operational. Check F1". To check or replace this fuse, follow this procedure:

Step 1: Power down the SCRIBE, open the system's front panel, and extract the MVME117 CPU board using the extraction procedure described in paragraph 4.9.3.

Step 2: Locate fuse F1 near the backplane edge of the CPU board, directly between backplane connectors P1 and P2. The board is silkscreened "F1", and it is socketed for easy replacement.

Step 3: Using a soldering pick or small screwdriver, gently extract the fuse.

Step 4: Check fuse continuity. If the fuse is good, replace it. Then, reinstall the CPU board.

Step 5. If the fuse is blown, check the SCSI connections, the transition board seating, and look for any damage or foreign material that may have caused the fuse to blow. Correct any problems if necessary.

Step 6. Replace the fuse with an axial, microminiature fuse with a rating of 1A/125 VDC. If you have difficulty obtaining such a fuse, please contact CHYRON Customer Service for assistance.

Step 7. Replace the MVME117 CPU board in the mainframe. Close the system's front panel, then power up the system and run diagnostics. If the fuse blows repeatedly, contact CHYRON Customer Service for further assistance.

6.3.3 PERIODIC SYSTEM DIAGNOSTICS

To operate the system diagnostics program, refer to Section IV of this manual. If you discover any errors through the diagnostics program, take corrective action and/or contact CHYRON Customer Service for assistance.

Section 7

SCRIBE SCHEMATICS CATALOG

7.1 GENERAL

This section provides a catalog of SCRIBE schematic diagrams. One complete set of schematics is supplied with each unit. This section, therefore, is a reference into the SCRIBE schematic diagrams.

7.2 LIST OF AVAILABLE SCHEMATICS

The following list contains all schematics and part numbers for the SCRIBE system:

Schematic Diagram Name	Number of sheets	CHYRON Part #
Keyboard Logics	2 sheets	C2A00842
Transition Board Logics	2 sheets	C2A00908
Dual Ported Memory Logics	7 sheets	C2A00941
BMPU Board Logics	12 sheets	C2A00859
Frame Buffer Logics	13 sheets	C2A00858
Analog Transition Board Logics	1 sheet	C2A00894
Display & Cursor Logics	12 sheets	C2A00869
Sync Generator Logics	11 sheets	C2A00935
Encoder Board Logics	11 sheets	C2A00936
Oscillator Board Logics	1 sheet	B2A00938

SCRIBE
EXTENDER BOARD

The following pages should be inserted into your SCRIBE Technical Manual at the end of Section 6.

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January, 1988

6.4 SCRIBE EXTENDER BOARD (OPTIONAL)

The SCRIBE Extender Board Assembly is composed of five pieces which can be combined to enable a technician to troubleshoot both 6U and 9U PC boards. The Extender Board Assembly is necessary for most troubleshooting procedures. All parts for the Extender Board are available individually from Chyron.

CAUTION

> **When installing or removing the Extender Assembly or a SCRIBE Board from the SCRIBE chassis, the SCRIBE must be off. Failure to remove power from the SCRIBE may result in equipment damage.**

You will need a small standard screwdriver to assemble the Extender Board. Before beginning board assembly, make sure all necessary hardware is present. You should have:

- One J1 Level Extender Board 243-26487G (Part No. 19C0014)
- Two J2 Level Extender Boards 243-26499H (Part No. 19C0015)
- Two Fiberglass Spacers (Part No. 19E0001)
- Eight screws (supplied)

CAUTION

> **When using the Extender Assembly, the J1 Level Extender Board must be above the J2 Level Extender Board during insertion into the SCRIBE chassis. Improper insertion may result in equipment damage.**

6.4.1 6U EXTENDER BOARD ASSEMBLY INSTRUCTIONS

The Extender Card can be assembled to accommodate a 6U PC board by following this procedure.

Step One: Place one Fiberglass Spacer (Part No. 19E0001) and the single J1 Level Extender Board 243-26487 (Part No. 19C0014) on a table, align the existing screw holes as shown in Figure 6-1

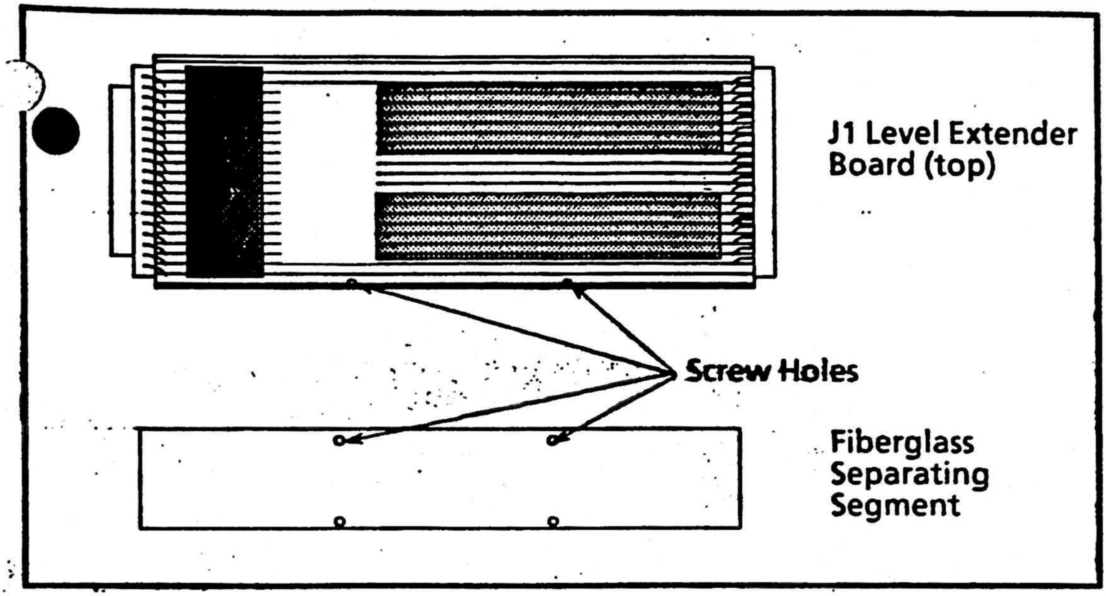

Figure 6-1. Initial Assembly

Step Two: Insert and tighten two of the supplied screws, connecting the J1 Level Extender Board 243-26487G (Part No. 19C0014) to the Fiberglass Spacer (Part No. 19E0001). When connecting these two pieces, make sure the Fiberglass Spacer is behind the J1 Level Extender Board 243-26487 (Part No. 19C0014).

Step Three: Place one of the J2 Level Extender Boards 244-26499 (Part No. 19C0015) over the attached Fiberglass Spacer, align the screw holes in each board, insert and tighten two of the supplied screws. Refer to Figure 6-2 for details.

Once both Extender Boards have been connected the board assembly can be used in troubleshooting 6U boards. To use the Extender Board Assembly, remove the board you wish to troubleshoot from the SCRIBE chassis, insert the Extender Board Assembly and attach the SCRIBE PC board to the Extender Board Assembly.

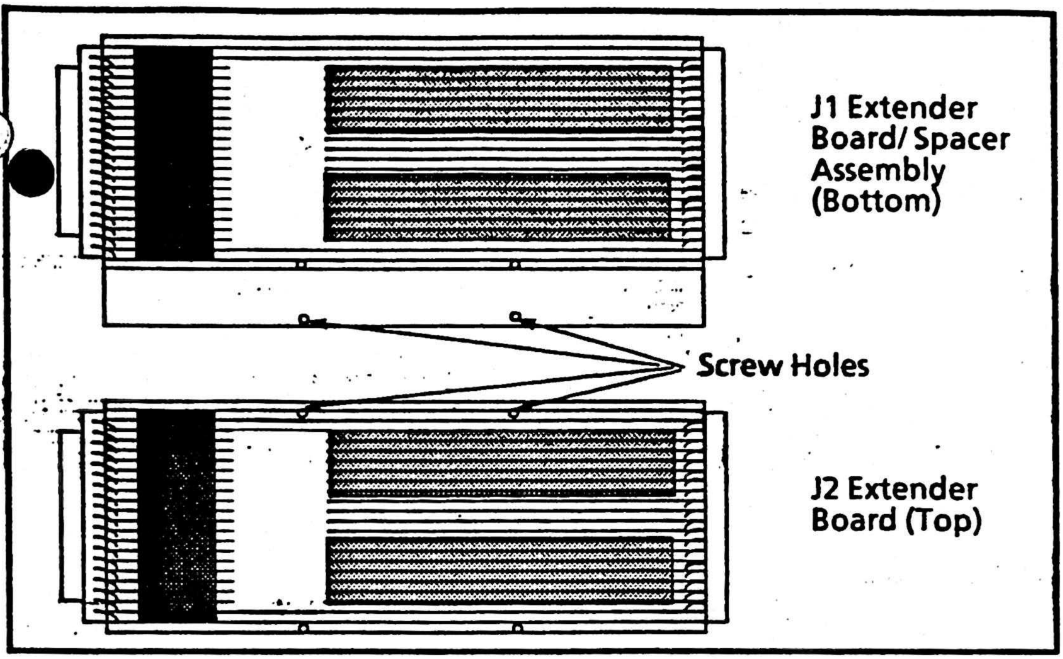

Figure 6-2. 6U Completion Assembly

6.4.2 9 U EXTENDER BOARD ASSEMBLY INSTRUCTIONS

The 6U Extender Board Assembly can be expanded to accommodate the larger 9U PC boards. The following procedure provides detailed assembly instructions.

Step One:	Construct the 6U Extender Board Assembly as previously described in paragraph 6.4.1. The completed assembly appears in Figure 6-3.
Step Two:	Align the screw holes for the J2 Level portion of the 6U Extender Board Assembly with the screw holes of the Fiberglass Spacer. Make sure the remaining Fiberglass Spacer is behind the 6U Extender Board Assembly. Refer to Figure 6-4 for details.
Step Three:	Place the remaining J2 Level Extender Board 244-26499 (Part No. 19C0015) on top of the attached Fiberglass Spacing Segment, align the screw holes, insert and tighten two of the supplied screws. Refer to Figure 6-5 for details.

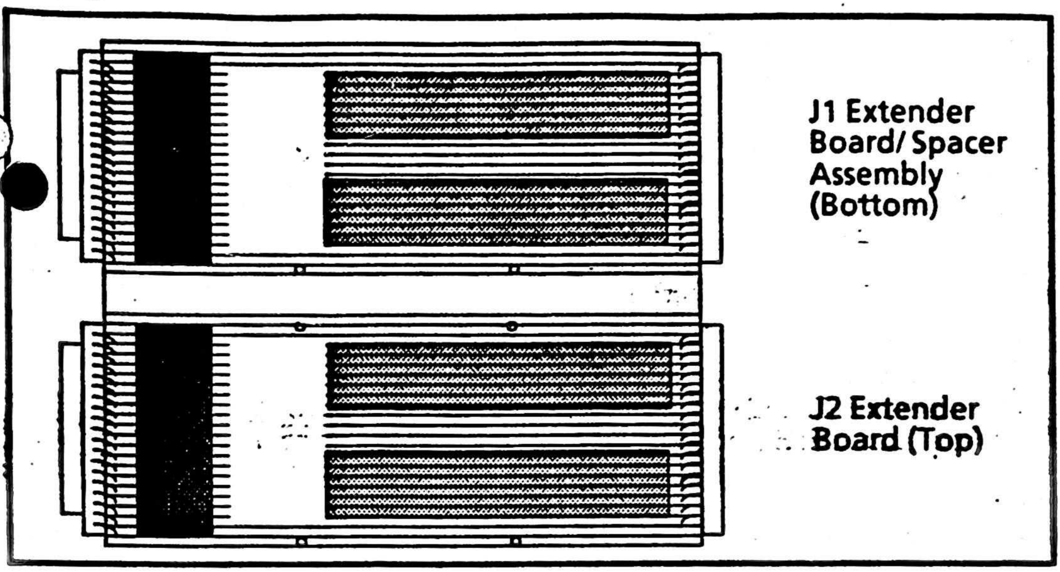
J1 Extender Board/ Spacer Assembly (Bottom)
J2 Extender Board (Top)

Figure 6-3. 6U Extender Board Assembly

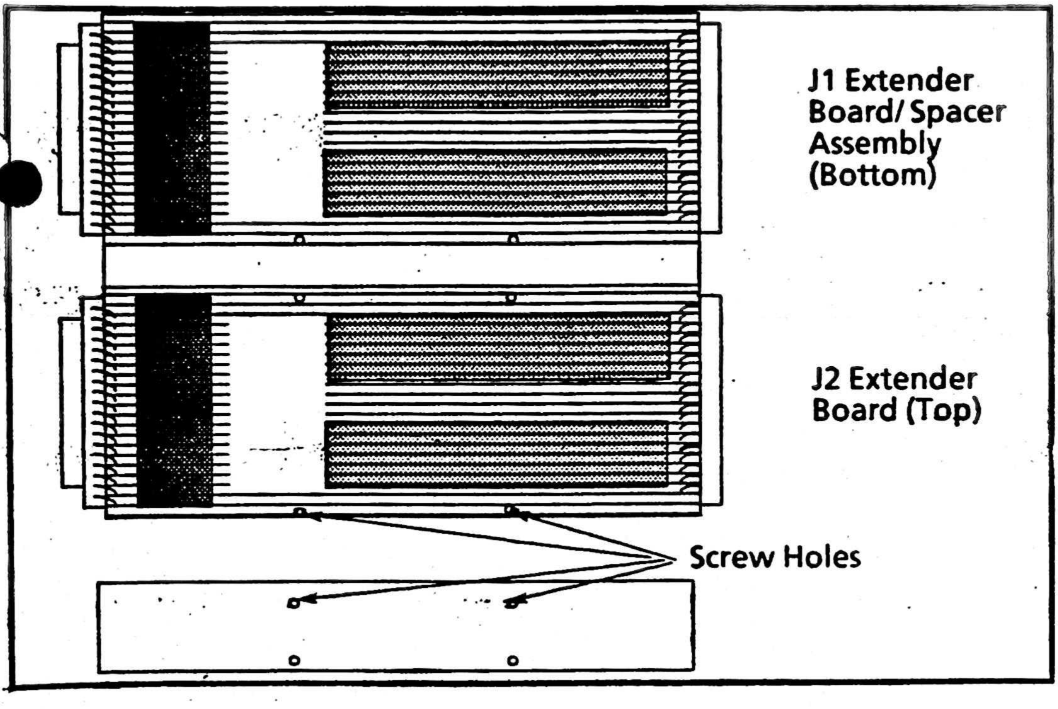
J1 Extender Board/ Spacer Assembly (Bottom)
J2 Extender Board (Top)
Screw Holes

Figure 6-4. 6U Extender Board Assembly

After the 9U Extender Board Assembly is constructed, the board can be [illegible]d to simplify troubleshooting of 9U P.C.Boards.

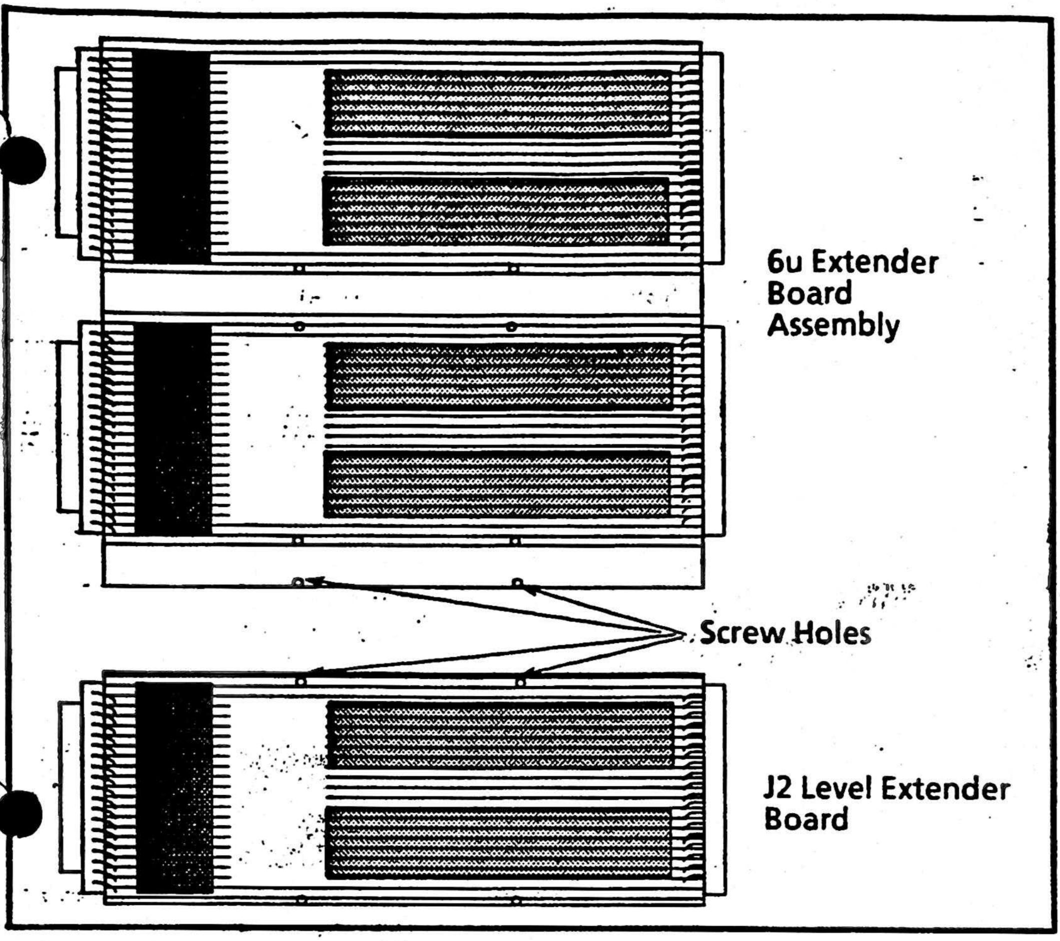
6u Extender Board Assembly
Screw Holes
J2 Level Extender Board

Figure 6-5. 6U Extender Board Assembly